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Self-Aligned Patterning Methods for Large-Area Electronics

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Self-Aligned Patterning Methods for Large-Area Electronics

Thesis for the degree of Doctor of Science in Technology to be presented with due permission for public examination and criticism in Tietotalo Building, Auditorium TB109, at Tampere University of Technology, on the 11th of December 2015, at 12 noon.

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Abstract

Printed electronics is studied as an alternative to conventional electrics, especially for large-area applications, such as organic light emitting diode (OLED) lighting panels. The whole technology, however, suffers from a low resolution and registration accuracy in the printing process, limitations that directly affect the performance of the applications. Photolithography can overcome these limitations and provide both good registration accuracy and resolution, but it is a challenging process in high throughput fabrication. Thus new fabrication methods are being studied intensively to replace expensive lithography steps in the fabrication chain.

This thesis presents two alternative fabrication methods with a scale-up capacity for high volume production. The first combines fast low-resolution patterning with roll-to-roll scalable high resolution microcutting; the second was developed to accurately align dielectric patterns on conductors. The latter uses an electric current to heat metal lines and cure a polymer dielectric locally near the conductor. Uncured polymer is rinsed away, leaving an aligned dielectric on the lines. The method is well suited for passivating OLED anode grid lines, which require excellent registration accuracy to prevent significant losses in the device active area.

The layer-to-layer registration accuracy of Joule heating is defined by heat conduction in the substrate. Thus the accuracy can be increased either by selecting a thermally low conductive substrate or by using short current pulses. The latter method allows more freedom to design the other process parameters and materials. An optimal pulse length depends on the substrate material in that materials with high thermal conductivity require short heating pulses. Here though the pulse lengths are of the order of milliseconds, which are easy to produce. In addition to increased registration accuracy, pulsed heating significantly cuts down the processing time and required energy.

In this thesis, a dielectric registration accuracy of 2 µm was demonstrated on shadow-mask-evaporated silver lines on glass, a value similar to that reported for registration accuracy in roll-to-roll photolithography, 1 µm. Joule heating, however, does not require challenging alignment steps. To demonstrate the feasibility of Joule heating for passivation in an OLED device, a printed silver current distribution grid was passivated using pulsed Joule heating and fabricated as an OLED device.

The Joule heating work constituted not only an experimental study but involved extensive finite element simulations to obtain design rules for the current distribution grid and to study the heating selectivity. The idea of the pulsed heating was also a result of this work.

Preface

This work was carried out at the Department of Electronics and Communications Engineering at Tampere University of Technology. The research was funded by UPM-Kymmene Corporation, the Finnish Funding Agency for Technology and Innovation (Tekes) and the European Union Seventh Framework Programme. The work was also supported by Tekniikan edistämissäätiö, Ulla Tuominen foundation, Jenny and Antti Wihuri Foundation and Nokia Foundation.

When I joined the Organic Electronics group, the background of the group was in organic rectifying diodes. There was an idea of a new fabrication method, which was given to me for realization. This work was in a new field for the group, thus I have met a lot of trouble in the way to this point. I am grateful to my supervisor Professor Donald Lupo for trusting me despite all the difficulties. My co-supervisor Assistant Professor Sampo Tuukkanen I would like to thank for his guidance and sharing the good, the bad, and the ugly moments from the beginning my thesis project. I wish also to thank all the co-authors of the publications and all my present and past co-workers, especially, Ph.D. Petri Heljo and M.Sc. Suvi Lehtimäki for the many helpful and pleasant conversations.

Most of all, I wish to thank my family for all their support and love, especially my little son Otso always cheering me up, and my dad and Erkka, with whom I have had the most fruitful conversations about my work.

Tampere, October 2015

Marika Janka

Contents

Symbols and abbreviations

γ	Material parameter in thermoelectric model
ρ	Density, $\mathrm{kg/m^3}$
C_p	Specific heat capacity, $\mathrm{J/(kg \cdot K)}$
d	Line pitch of a current distribution grid, m
DC	Direct current
F	Mapping between modelling domains
FEM	Finite element method
I	Electric current, A
ITO	Indium-tin oxide
J	Jacobian matrix
k	Thermal conductivity, $\mathrm{W/(m \cdot K)}$
NIL	Nanoimprint lithography
OFET	Organic field-effect transistor
OLED	Organic light emitting diode
OPV	Organic photovoltaic
PET	Polyethylene terephthalate
PGMEA	Propylene glycol monomethyl ether acetate
PVP	Poly(4-vinylphenol)
Q	Thermal power density $\mathrm{W/m^3}$
q	Heat flux, $\mathrm{W/m^2}$
R	Electrical resistance, Ω
R_{sheet}	Sheet resistance, $\Omega/\square$
SEM	Scanning electrode microscopy
T	Temperature, K
T_0	Temperature at the line edge, K
T_{CL}	Minimum temperature at which cross-linking takes place, K
t	Time, s
v	Volume, $\mathrm{m^3}$
x	Distance from grid line edge, m
x_{OH}	Dielectric overhang, m

List of publications

Paper 1 M. Janka, S. Tuukkanen, T. Joutsenoja, and D. Lupo. Self-Alignment Method for Solution-Processable Dielectric Structures via Joule Heating. *Thin Solid Films*, 519(19):6587–6590,2011.

Paper 2 M. Janka, P. Raumonen, S. Tuukkanen, and D. Lupo. Modelling of Joule heating based self-alignment method for metal grid line passivation. *MRS Proceedings* 1628, 2014.

Paper 3 M. Janka,E. Saukko, P. Raumonen, and D. Lupo. Optimization of large-area OLED current distribution grids with self-aligned passivation. *Organic Electronics* 15(12):3431–3438, 2014.

Paper 4 M. Janka, R. Gierth, J.-E. Rubingh, M. Abendroth, M. Eggert, D.J.D. Moet, and D. Lupo. Passivation of OLED anode grid lines by pulsed Joule heating. *Applied Physics Letters* 107(10):103304, 2015.

Paper 5 M. Janka, S. Tuukkanen, H. Tuorila, J. Viheriälä, M. Honkanen, N. Stingelin, D. Lupo. Use of microcutting for high throughput electrode patterning on a flexible substrate. *Journal of Micromechanics and Microengineering* 24(1):015015, 2014.

1 Introduction

Printed electronics is based on the idea of the letterpress, which is designed to decrease the cost and increase the production volume of books and papers. The discovery of a polymer whose conductivity can be varied by doping was the first step toward printed electronics (Chiang et al., 1977; Heeger, 2001). The processability of these polymers into solvent-based inks enables use of conventional printing techniques in electronics. The idea behind the technology is equivalent to conventional graphics printing, but the colours in graphics printing exploit the different electrical properties of materials. Whereas the required resolution in graphics printing is determined by the resolution of the human eye, in printed electronics the functionality of the devices and circuits necessitate higher resolution.

Here some printing techniques and their limitations are discussed. Along with the application and material properties, the aimed production quantity defines the optimal printing method, and resolution and layer-to-layer registration accuracy define the performance of the fabricated devices. For example, the performance of printed transistors usually suffers from the low resolution and poor registration accuracy of the printing processes, leading to large channel length and high overlap capacitance. The same printing technique limitations also lower the performance of other applications, such as large-area OLEDs and displays, which require accurate deposition of material. Layer-to-layer registration accuracy of the process defines the misalignment of subsequent layers. Furthermore, if the full coverage of the underlying layer is required, the width of the second layer pattern need to be increased to twice the registration accuracy of the process. The term overhang used in this dissertation means the length of the top layer that exceeds the layer below. Thus the mean overhang corresponds to the registration accuracy of the process (see Figure 1.1).

Screen printing is a contact printing method whereby ink is imprinted through a patterned mesh with a squeegee. The process requires highly viscous inks to reduce ink spread on the substrate. (Cantatore, 2013; Subramanian et al., 2008) To achieve such high viscosity, high ink solid content or optionally suitable additives are required, the former resulting in thick dry films. (Cantatore, 2013, p.36) Consequently, screen printing is an optimal method for applications that require thick and highly conductive electrodes, such as RFID antennas (Virkki et al., 2014) and current distribution grids for organic photovoltaic (OPV) (Galagan et al., 2011) and organic light emitting diodes (OLEDs). However, like other printing techniques, screen printing suffers from relatively poor layer-to-layer registration accuracy, 25 µm (Guerin et al., 2011), and resolution, about 50 µm (Tobjörk and Österbacka, 2011).

Along with screen printing, gravure is a conventional printing technique. Printed patterns are engraved in a metal plate or a cylinder, which is then rolled over a moving substrate.

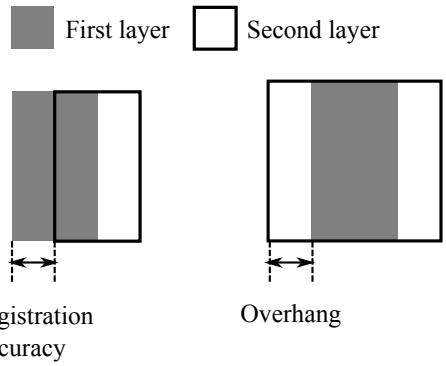

Figure 1.1: Definition of registration accuracy and overhang. To guarantee full coverage of the underlying layer the second layer has to be twice the registration accuracy wider than the under lying layer. The overhang is the measure the second layer exceeds the underlying layer, which correspond the registration accuracy

Ink is deposited over the cylinder, from which a doctor blade wipes off the excess, simultaneously filling the engraved patterns. (Sung et al., 2010) Though gravure rolls have long lifetimes, they are expensive to fabricate. Thus gravure printing is used only for high volumes. It is a high-throughput process suitable for a wide range of materials (Ding et al., 2009; Heljo et al., 2014; Puetz and Aegerter, 2008), thus enabling fabrication of various applications, such as organic rectifying diodes, OLEDs, OPVs, and organic field-effect transistors (OFETs) (Hassinen and Sandberg, 2013; Kopola et al., 2009; Lilja et al., 2009; Voigt et al., 2012). Its printing resolution is about 20 µm (Tobjörk and Österbacka, 2011) and its registration accuracy 16 µm perpendicular and 40 µm parallel to the printing direction (Noh et al., 2010)

Inkjet is a digital printing technique that requires no physical masters. The printed pattern can thus be easily modified only by the digital image. This method is a non-contact printing method, whereby individual small-volume droplets are directed to the substrate to form patterns defined by the digital image. Statistical variations in the flight direction of droplets and their spreading on the substrate limit the printing resolution to 20 to 50 µm (Sirringhaus et al., 2000). The same parameters define the layer-to-layer registration accuracy, which is 15 µm (Ng et al., 2012).

Though roll-to-roll photolithography is not a printing method, it is reviewed here as an alternative to printing when high resolution and registration accuracies are required. Roll-to-roll photolithography is, however, a more complicated and inaccurate process than photolithography, which is targeted for rigid substrates. Because flexible substrates are dimensionally relatively unstable, thermal expansion, shrinkage, and substrate deformation during handling cause misalignment between the deposited layers. Commonly, individual photomasks for each layer are needed to compensate for dimensional distortion. (Zhang et al., 2010) Mechanical and mathematical models are also essential to reduce the misalignment of the layers. (Gleskova et al., 2006) Whereas in printing only two process steps are necessary – deposition and curing the patterns – at least resist deposition, exposure, rinsing, and development steps are needed in photolithography (Zhang et al., 2010), though depending on the application, lift-off or etching and resist removal may also be required. Thus photolithography is a relatively expensive and challenging process. However, its resolution is only a few microns and its layer-to-layer alignment accuracy

only about 1 µm (Zhang et al., 2010), which is more than an order of magnitude smaller than can be achieved with printing methods.

To improve the economic feasibility of printed electronics, alternative high resolution patterning techniques have been developed. Nanoimprint lithography (NIL) is one of these new approaches. The advantages of NIL are its capability to achieve extremely high resolution beyond the limitations set by light diffraction or beam scattering and its transferability into a continuous roll-to-roll process. The process consists of the following steps: the resist is applied over the substrate, followed by imprinting of the resist with a patterned roller and UV curing. (Ahn and Guo, 2009) Depending on the application, imprinting can be followed by process stages common in conventional photolithography, such as etching and lift-off. (Guo, 2007) Like photolithography, NIL requires additional alignment steps when multiple layers are deposited.

A different approach is to increase resolution or registration accuracy by combining printing and self-alignment methods. Many different techniques have been studied to downscale the feature separation. A high separation resolution can be achieved, for example, by inducing ink repulsion from the previously deposited layer by modifying the surface energy of the previous electrodes (Sele et al., 2005; Zhao et al., 2007) or by patterning a hydrophilic substrate with hydrophobic surface regions. (Sirringhaus et al., 2000) However, the layer-to-layer registration accuracy has attracted less attention. A top-gate transistor structure with minimal parasitic overlap capacitance was demonstrated by using a self-aligned source and drain electrode as a photomask and backside illumination to define the gate electrode (Noh et al., 2007). Another approach to decrease the overlap of electrodes is to self-align the source and the drain to the gate by using a wetting-based roll-off technique. (Tseng and Subramanian, 2011) All the above techniques have been developed for the requirements of the printed transistor.

Recently, serious investments have been made to utilize large-area OLED lighting in mass production. Little attention, however, has been paid to passivating the OLED current distribution grid, despite the fact that the alignment accuracy of the passivation layer is one key factor that defines the performance of the device. The above self-alignment methods are not compatible with current distribution grids, because instead of avoiding the overlap of successive layers, as in the transistor application, the passivation layer must fully cover the grid lines with minimal overhang.

1.1 Aim and scope

As described above, for some electronic applications the printing processes do not allow high enough resolution and layer-to-layer registration accuracies. Though roll-to-roll scalable high-resolution fabrication methods have lately been extensively studied, new methods are still necessary. Moreover, most new methods to date concentrate on minimizing the overlap of the adjacent layers or on creating high resolution patterns. Accurate overlay alignment has drawn much less attention.

This thesis focuses on two fabrication techniques: a *Joule-heating-based alignment method* for solution processable dielectrics and *microcutting* for patterning high resolution electrodes. The former aims to improve the layer-to-layer registration accuracy of the dielectric pattern on target conductors and the latter to pattern and align adjacent high resolution conductors. Combining both methods enables patterning of lateral transistor electrodes and aligning the gate dielectric on the gate. The Joule-heating-based alignment method

was initially designed to pattern dielectric onto the microcut electrodes, but it was later developed into a processing technique for OLED anode passivation.

The microcutting work here followed the pioneering work of Natalie Stingeling(-Stutzmann), though the pattern design was new. Joule heating, however, as far as the author knows, has not been studied before for passivation. Commonly treated as a disadvantageous side effect in electronic application, but it has yet been used to ablate polymer from silicon nanowires in a self-aligned manner. (Park et al., 2007)

The basis of the study described earlier led to the following seminal scientific questions justifying this work:

- What are the limitations of microcutting in electrode patterning?
- What are the theoretical underlying limitations of the Joule heating method?
- What are the possibilities of Joule heating for polymer film curing and localization?
- What are the limitations of Joule heating in grid design?

1.2 Structure of the Thesis

This compendium of the thesis outlines the work presented in five peer-reviewed articles, yet it is independent and does not follow the structure of the publications. Some results presented in this thesis not previously published have been selected to give a better view of the subject.

The main focus of the thesis is the Joule-heating-based self-alignment method for dielectric patterning. The method is first introduced in **Paper 1**, and **Paper 2** and **Paper 3** present a detailed simulations of the method. At the beginning of Chapter 2, the Joule heating method and one to model the Joule heating phenomenon are described. The phenomenon itself is discussed together with modelling results. At the end of the chapter, pulsed Joule heating and its advantages are introduced. The chapter describes the evolution of understanding the Joule heating process gained during this thesis project.

Chapter 3 is devoted to the main application of the Joule heating method: passivation of a large-area OLED current distribution grid. The chapter begins with design rules for the current distribution grid (**Paper 3**) and ends with passivated anode grids. The highlight of the study was the fabrication of an OLED on printed anode grid lines passivated with the new pulsed Joule heating method. (**Paper 4**)

Chapter 4 presents a study of microcutting metal electrodes using two methods: hot embossing and imprinting at room temperature. Microcutting was used to pattern and precisely align narrow planar electrodes, and Joule heating, discussed in earlier chapters, was used to passivate microcut electrodes. The resulting pattern formed a thin film transistor (TFT) platform. The method combined coarse patterning, followed by high resolution microcutting. Both patterning steps are scalable to roll-to-roll manufacturing. (**Paper 5**)

The final chapter summarizes the work and provides an outlook of future improvements.

1.3 Author's contribution

The publications constituting the scientific output of this thesis are the results of collaboration. The author's contribution is defined as follows:

Paper 1: This paper presents a proof-of-concept of the Joule heating-based self-alignment method. The idea of the method derived from T. Joutsenoja, but the author designed its realization and primarily planned the experiments. She conducted them all except for the AFM measurements, which were conducted by S. Tuukkanen. The author wrote the first draft of the manuscript and revised it with the co-authors.

Paper 2: This paper studies through simulations the effect of substrate materials on the alignment accuracy of Joule heating. The author planned and carried out the modelling work. P. Raumonen helped transform the model into a scaled equivalent problem. The author wrote the first draft of the publication and revised it with the co-authors.

Paper 3: This paper continues the work presented in **Paper 2**. It describes the Joule heating process and the factors affecting the alignment accuracy. The paper also presents the design rules for a current distribution grid placed by Joule heating. The author planned and carried out the modelling work, but the OLED luminance model was built together with E. Saukko. The author wrote the first draft of the publication and revised it with the co-authors.

Paper 4: This paper presents an improved Joule heating setup and improvements on registration accuracy by modelling. Theoretical results are qualified experimentally. Finally, the feasibility of printed grid lines and Joule-heating-based passivation are demonstrated in an OLED device. The author conceived the idea of pulsed Joule heating and planned and carried out the Joule heating and modelling work. R. Gierth and J.-E. Rubingh designed the OLED and the current distribution grid. J.-E. Rubingh printed the grid, and R. Gierth fabricated the OLED. The author wrote the first draft of the publication, except for the paragraphs on OLEDs and printing of the grids. The manuscript was revised with the co-authors.

Paper 5: In this paper, the author primarily planned the experiments and did all the microcutting and Joule heating work. J. Viheriälä and H. Tuorila fabricated the stamps used in the experiments. The SEM images were taken by H. Tuorila and M. Honkanen. The author wrote the manuscript, except for the introduction and the paragraph on stamp manufacturing. The manuscript was revised with co-authors.

2 Joule-heating-based self-alignment method for dielectric structures

Joule heating is used to locally heat conducting structures with an electric current. The Joule heating method can be used to precisely align thermally curable dielectric layers to metal patterns (process illustrated in Figure 2.1). In the first stage of the process, a thermally cross-linkable polymer is applied on a conductor. The conductor is then heated selectively with an electric current passing through the metal line, while the polymer cross-links near the grid lines. Finally, the non-cross-linked soluble dielectric is rinsed away, leaving an aligned dielectric pattern on the conductor. The length of the dielectric layer exceeding the line edge is called overhang (x_{OH}), and it defines the registration of the process. (**Paper 1**)

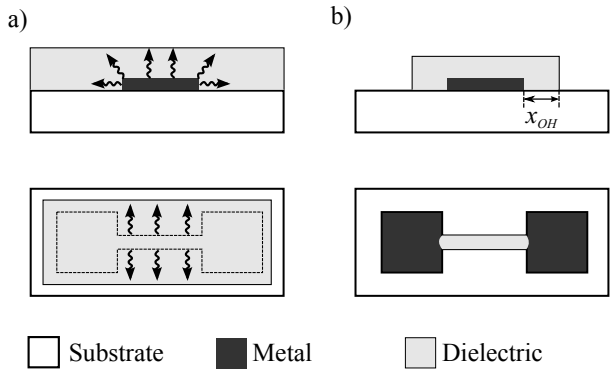

Figure 2.1: Joule heating process. a) A thermally cross-linkable polymer dielectric is heated using an electric current passing through the conductor. b) Subsequently, any uncured dielectric is removed by rinsing the substrate with a solvent, resulting in an aligned dielectric layer on top of the conductor. The dielectric overhang (x_{OH}) defines the alignment accuracy. Adapted from **Paper 1**.

A very promising application for Joule-heating-based self-alignment is passivation of the current distribution grids, which are needed in large-area organic light emitting diodes (OLED) and organic photovoltaic (OPV) applications. The grid increases the conductivity of an anode and thus increases the performance of the device.

This chapter deals with the basic phenomena behind Joule heating and factors affecting the accuracy of registration. Because modelling the Joule heating process is an important part of this thesis, and because it has contributed to a deeper understanding of the

process, the method is described at the beginning of the next section, and the theory behind the phenomenon and the results are presented together.

2.1 Modelling method

For this dissertation, the Joule heating process was studied by finite element modelling (Comsol 4.3 from Comsol, Inc). The modelled system consisted of domains with large dimensional differences: in width and height, the grid lines were from two to five orders of magnitude smaller than in length. Furthermore, the grid systems consisted of several lines. Consequently, modelling such a geometry would have resulted in a very large mesh (finite element mesh, which is division of the domain of the problem into a collection of subdomains), which would either have added significantly to the modelling time or a mesh may not have been generated at all. To reduce the modelling time, the process was divided into two submodels: a two-dimensional current model to study the current on a grid scale, and a three-dimensional thermoelectric model to estimate the locality of the heating in a small subsection of the grid. (**Paper 3**) The modelling procedure is shown in Figure 2.2.

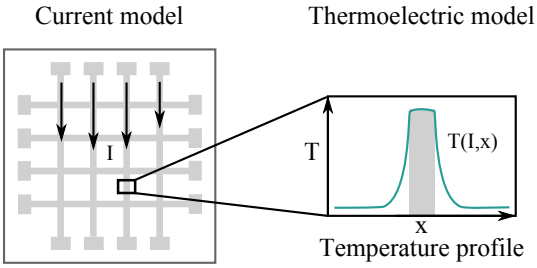

Figure 2.2: The Joule heating model was divided into two submodels: a current model of the grid system to compare current flow in a different grid design and a thermoelectric model of subsections of the grid.

To reduce the dimensional differences in the standard geometry of the system, the thermoelectric problem was described using an equivalent problem with a scaled geometry. (Raumonen et al., 2008, **Paper 2**) Figure 2.3 a) shows the modelling geometry used in the thermoelectric model, and the scaling of the geometrical dimensions is described in Figure 2.3 b). Mathematically, the original problem was transformed into a new geometry using a mapping F between the domains:

$$\mathbf{x_1} = F(\mathbf{x_0}) \tag{2.1}$$

To make the new problem equivalent to the original problem, materials parameters had to be modified with the Jacobian matrix J of the mapping F. (Raumonen et al., 2008)

$$\gamma_1 = \frac{1}{\det(J)} J \gamma_0 J^T, \tag{2.2}$$

where γ presents material parameter matrices in the domains, and $\det(J)$ and J^T are the determinant and the transpose of the Jacobian matrix, respectively. Notice that the mapping need only be continuous and piecewise differentiable.

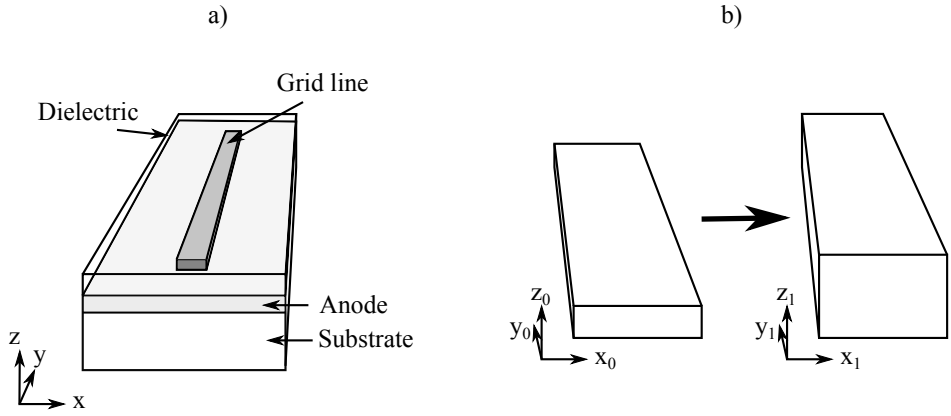

Figure 2.3: a) The geometry used in the thermoelectric model (dimensions not to scale) and b) scaling of the geometrical dimensions. (**Paper 2**)

2.2 Stationary equations and DC heating

In 1841, James Prescott Joule discovered the heating effect of an electric current and came to the conclusion that "when a current of voltaic electricity is propagated along a metallic conductor, the heat evolved in a given time is proportional to the resistance of the conductor multiplied by the square of the electric intensity." (Joule, 1841) In unit volume, this can be presented as follows:

$$Q \propto \frac{RI^2}{v}, \tag{2.3}$$

where Q is the thermal power density, R is the resistance, I is the electric current, v is the volume. In a Joule heating process, heat is generated in a conductor, from where it is conducted to a substrate and dielectric. Natural convection transports the heat from the dielectric surface to ambient air, but for the self-alignment method, conduction in solids is the key for defining the registration accuracy of the process; hence, the discussion here concentrates on conduction. In a solid material, heat conduction can be described by the Fourier law of heat conduction:

$$-k\nabla T = q, \tag{2.4}$$

where q is the heat flux, k is the thermal conductivity, and ∇T the temperature gradient. (Fourier, 1878). According to the energy conservation law: the energy generated in a conductor and heat flux density are equal. In a stationary situation, this can be presented as:

$$-\nabla \cdot (k\nabla T) = Q. \tag{2.5}$$

From Equation 2.5 it can be conclude that a small spatial temperature gradient is created in materials with high thermal conductivity. This means that the higher the thermal conductivity, the larger the heated area, and thus more energy is needed to heat up the grid lines.

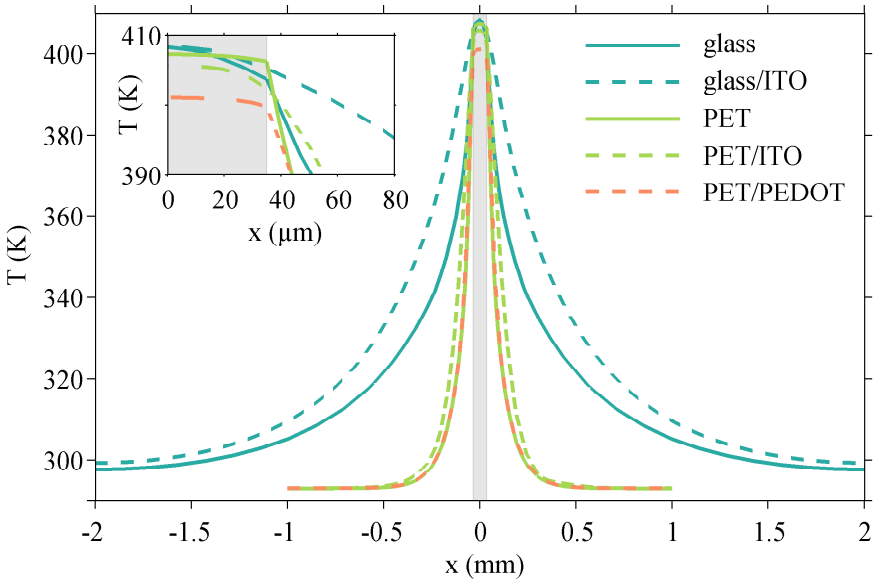

Figure 2.4: The effect of substrate thermal conductivity on heat conduction. (glass I=390 mA, glass/ITO I=530 mA, PET I=180 mA, PET/ITO I=220 mA, PET/PEDOT I=180 mA) Adapted from (**Paper 2**, **Paper 3**)

The above behaviour was confirmed by modelling. Table 2.1 shows the material parameters used in the model, and Figure 2.4 the modelled temperature distribution across a 500 nm thick and 70 µm wide aluminium conductor. Glass and PET substrates were compared to study the effect of the substrate material on the selectivity of heating. Modelling was repeated with an ITO layer on both substrates and a poly(3,4-ethylenedixythiophene) poly(stryrenesulfonate) (PEDOT:PSS) layer on the PET substrate. The heating current was selected to induce a temperature of 410 K at the grid line, which is close to the cross-linking temperature of the polymers used in the experiments when the heating time is in the order of minutes. (**Paper 2**, **Paper 3**)

Table 2.1: Material parameters used in the model. The original thickness of the material is denoted by h_0 and the scaled thickness by h_1.

Material	h_0 (µm)	h_1 (µm)	k (W/(m · K))	R_{sheet} (Ω/□)
PET	125	125	0.15 (Brandrup et al., 1999)	-
Glass	1000	1000	1.4 (Rohsenow et al., 1998)	-
PEDOT:PSS	0.1	50 µm	0.17 (Feng-Xing et al., 2008)	200
ITO	0.15	50 µm	10.2 (Thuau et al., 2011)	14

During Joule heating, heat conduction along the glass substrate was significant when compared to the PET substrate. Thus the power needed to reach 410 K on the PET substrate was only 21% of that used to heat glass. The difference is explained by the 10 times higher thermal conductivity of glass over PET (Brandrup et al., 1999; Rohsenow et al., 1998). However, evaluating only the amount of heat dissipated into a substrate does not realistically describe the selectivity of heating. A better proxy is the temperature gradient at the edge of the conductor. The faster the temperature decreases

in the substrate, the less small variations in temperature affect the size of the dielectric overhang.

The temperature gradient for the glass substrates was approximately 1 K/µm, whereas for PET it was about 2 K/µm. This means, as expected, a lower heating selectivity for a glass than a PET substrate. (**Paper 2**) When ITO was applied to a substrate, it decreased the heat locality, as can be seen in the inset of Figure 2.4. Thus at the edge of the conductor, the selectivity dropped to 0.6 K/µm with the PET substrate and to 0.2 K/µm with the glass substrate. (**Paper 2**) Applying ITO onto a PET substrate increased the required current by 30 mA, due to both increased heat spreading into the substrate and the 16-mA current flowing in ITO. The current in ITO had a negligible heating effect due its low density. (**Paper 2**, **Paper 3**) When a 100-nm thick PEDOT:PSS layer was applied to the PET substrate, the maximum temperature dropped to 401 K, resulting from a small 1-mA current flowing in the transparent conductor. A PEDOT:PSS layer has no effect on localization, because the thermal conductivities of PET and PEDOT:PSS are similar (Brandrup et al., 1999; Feng-Xing et al., 2008). (**Paper 2**, **Paper 3**)

Though ITO has a 100 times higher thermal conductivity than PET (Brandrup et al., 1999; Thuau et al., 2011), the effect on heat diffusion into the substrate was less than might be expected. Because the thin ITO layer had a smaller cross-sectional area than the surface area of the conductor, heat flux along ITO was smaller than in the thick substrate and dielectric. (**Paper 2**, **Paper 3**)

The selection of substrate materials is not the only way to adjust the heating selectivity. Figure 2.5 shows a temperature gradient at the edge of the conductor as a function of thickness for a printed and an evaporated line. The cross-section of the printed line was modelled with a half ellipse and the evaporated one with a rectangular shape. In all simulations, the dielectric thickness is 6 µm, and the gradient was calculated in five locations for variance. Since the results vary only slightly, the error bars are not visible at all data points. (**Paper 3**)

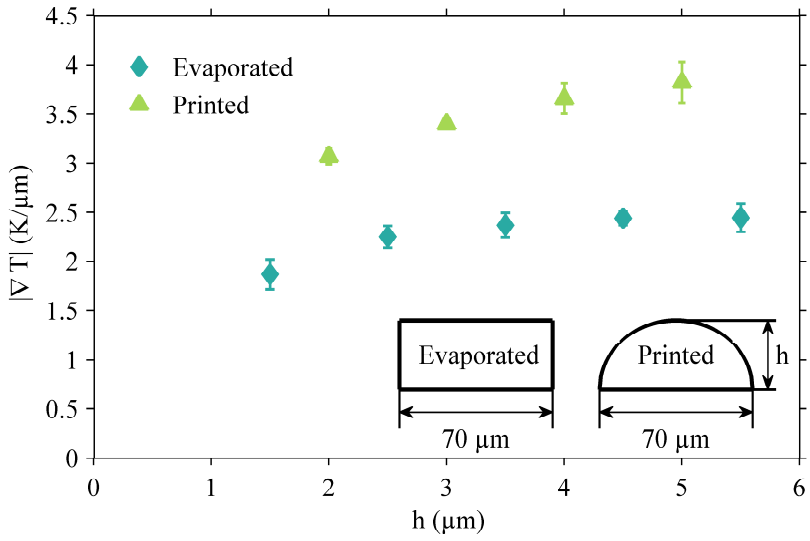

Figure 2.5: The effect of the line cross-section on heating selectivity. (**Paper 3**)

As can be seen in Figure 2.5, the shape of the conductor affects the gradient more than its thickness. Consequently, the size of the overhang is not as prone to changes in its cross-sectional area for printed lines as it is for evaporated lines. (**Paper 3**) However, because of inaccuracies in the printing processes, the printed lines vary more in their cross-sectional area than the evaporated lines.

The stationary equations and results presented in this section are valid when the heating time is longer than 0.3 s. The results leads us to conclude that the materials have a significant effect on the registration accuracy of the Joule heating process. Plastics are an ideal choice for substrate material for Joule heating, whereas glass is challenging due to its high thermal conductivity. Though plastics are ideal substrate materials in flexible electronics applications, they suffer from rapid water and oxygen permeation through the film, whereas glass has adequate barrier properties. In OLED operation, water and oxygen permeation leads to significantly shorter operating lifetime of device. Thus plastic substrates require encapsulation. (Burrows et al., 2001; Charton et al., 2006) However, to date, no commercially available encapsulation systems meet the requirements for water and oxygen permeation (Tsai et al., 2015). Thus in some applications, glass remains the preferred substrate material.

To make Joule heating more attractive for a wide range of applications, the effect of substrate thermal conductivity must be minimized. This is possible by limiting heat transfer from conductor to substrate, which improves the registration accuracy of the process.

2.3 Time-dependent heat conduction and pulse heating

The time-dependent equation for heat conduction in a solid medium is given by the equation

$$\rho C_p \frac{\partial T}{\partial t} = \nabla \cdot (k \nabla T) + Q, \tag{2.6}$$

where C_p is the specific heat capacity, ρ is the density, k is the thermal conductivity, and Q is the thermal power density (Samarskii and Vabishchevich, 1995). Before the system reaches its equilibrium, increase in heating time increases the heated area. Thus it is possible to limit the thermal diffusion in the substrate, by using short heat pulses.

The effect of pulse length on heating selectivity was studied with a time-dependent thermo-electric model for a 500-nm thick silver line on a PET- and an ITO-coated PET substrate. Figure 2.6 shows temperature gradient as a function of current pulse length and the inset the temperature profile from the middle of the line to the substrate and the location where the temperature gradient was calculated. The temperature gradient remains constant until pulse duration drops below 0.1 s. Below that, selectivity rises exponentially. With the ITO-coated PET substrate, the increase in gradient size is slower than with the plain PET substrate.

In addition to increased localization as curing time decreases, it is possible to increase localization also by using higher curing temperatures. Figure 2.6 shows curing selectivity for two grid temperatures for both substrates. The temperature T_m is the maximum calculated in the middle of the line.

The reproducibility of the process is defined by sensitivity of the size of the dielectric overhang on small changes in temperature at a grid line. Therefore a dependence of the overhang on the temperature at the line at constant curing time was derived. At

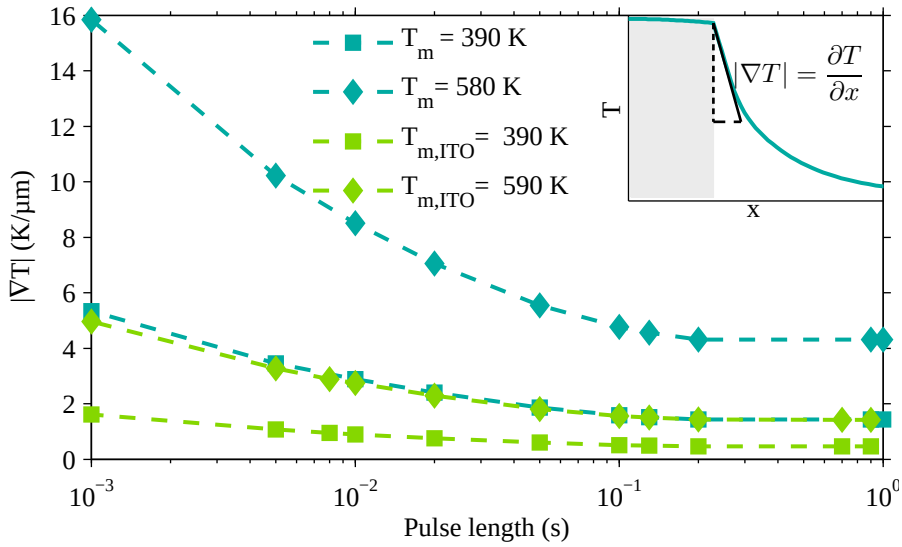

Figure 2.6: The modelled effect of pulse length on the temperature gradient at the edge of the line. Inset: Calculation of the temperature gradient from the temperature profile. Adapted from **Paper 4**.

the substrate, close to the line edge, temperature decreases linearly as a function of the distance x. Thus at small x the temperature in the substrate can be described as a function of the distance:

$$T(x) = T_0 - |\nabla T|x, \tag{2.7}$$

where T_0 and $|\nabla T|$ are the temperature and the temperature gradient at the line edge. The size of the dielectric overhang x_{OH} is the distance where temperature reaches T_{CL}, the minimum temperature at which the cross-linking takes place. This temperature can be defined as

$$T_{CL} = T_0 - |\nabla T|x_{OH}. \tag{2.8}$$

Because at constant curing time the cross-linking temperature T_{CL} is constant, the relation between the change in the temperature at the line edge ΔT_0 and the change in the overhang Δx_{OH} can be described as

$$\Delta T_0 = |\nabla T|\Delta x_{OH}. \tag{2.9}$$

Though the equation is a simplification and is valid only when ΔT_0 is small (tens of Kelvins), it gives an estimate of how the overhang behaves when the curing temperature changes. From Equation 2.9 it can be concluded that if the temperature gradient at the edge of the line is high, the increase in the overhang is very small even if the temperature at the line increases. Therefore, with short pulses the size of the overhang is only slightly dependent on the changes in temperature. (Supporting information from **Paper 4**)

The increase in overhang (Δx_{OH}), according to Equation 2.9, gives a qualitative estimate of the temperature gradient at the edge of the line. Furthermore it is a quantity that is easy to measure. To verify the model data experimentally a series of 100-nm thick silver electrodes with a current choke in the centre of the line were designed. The electrodes were shadow-mask-evaporated on the PET substrate. A thermally cross-linkable polymer

(Bectron AL14-018H2 from ELANTAS Beck GmbH) was spin-coated on the substrate and subsequently cured by pulsed heating. The experiment was repeated with different choke widths and pulse durations: 1-min DC current, 100-ms, 50-ms, 10-ms pulsed current (detailed curing parameters are shown in Table 2.2). The number of pulses and current was selected for each pulse length to obtain full dielectric coverage of the electrode without damaging the substrate. Because the current density was higher at the choke than elsewhere, the temperature rose locally.

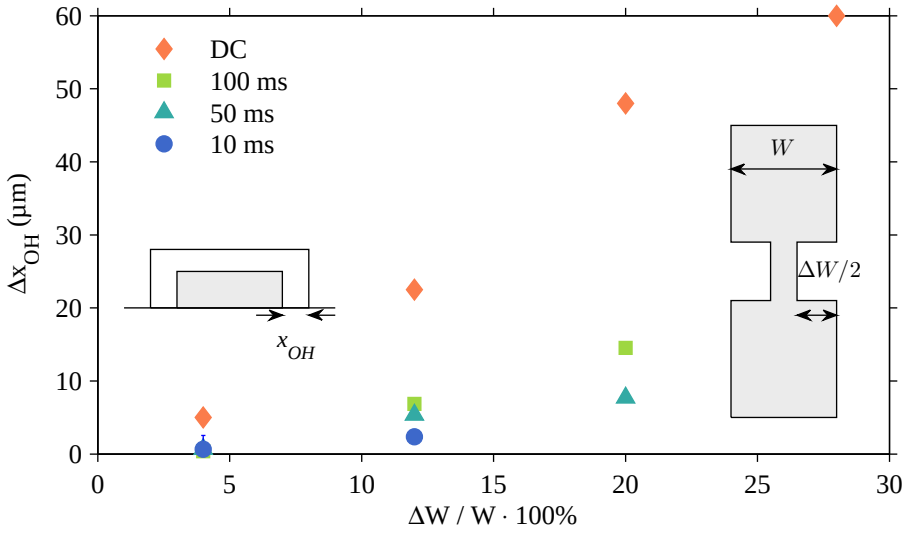

Figure 2.7: Increase in the dielectric overhang (x_{OH}) as a function of the difference in line width (W) and choke width ($W - \Delta W$). With a short pulse length, the size of the dielectric overhang is less prone to changes in line width. The schematics of the test pattern and a cross-section of the passivated line are shown in the insets. Adapted from **Paper 4**

Figure 2.7 shows the increase in the dielectric overhang Δx_{OH} due to the choke as a function of difference in width ΔW. The results show clearly that decreasing the pulse length increases the heating selectivity, though with pulsed heating the substrate under the choke melted earlier than with a DC current. Therefore, fewer measurement points are shown for pulsed than for DC heating. However, the results in Figure 2.7 show a more dramatic increase in the overhang and moreover the melting of the substrate takes place at smaller differences in line width than expected in passivation process. At the choke, the temperature increases as the length of the choke increases until it saturates. The length of the choke was selected to be 1 mm, which corresponds the saturation length during constant current heating. Typically, the grid line cross-sectional area varies in length in tens of micrometres rather than millimetres. (**Paper 4**)

In contrast the modelling data in Figure 2.6, the experiments showed significant increases in localization from DC curing to 100-ms pulse curing. The effect is not only caused by the decreased heat conduction into substrate by decreasing the heating time, but also the shorter the current pulse is the higher temperature at the conductor can be used without melting the underlying substrate. As can be concluded from the modelling data, increasing the temperature increases the localization as well. In conclusion, the following are two additional effects that increase localization when pulsed heating is applied: limited heat conduction into the substrate due to pulsed heating and increased temperature at

the conductor. In addition to increased localization, pulsed heating decreases the process time, because the higher the curing temperature, the faster the cross linking takes place. (**Paper 4**)

In addition to registration, energy consumption is an important parameter as regards process scalability to high volume production. Thus Table 2.2 shows the energy consumption data along with the curing parameters for the experiments in Figure 2.7. The resistance of the electrode was about 4.5 Ω. With a pulsed heating setup, energy consumption is significantly lower than with DC current heating simply because less heat is dissipated in the substrate than with DC heating. The lowest energy consumption was achieved with a 100-ms pulse. Optimization of the pulse energy depends on dimensional stability of the substrate and conductor at elevated temperatures as well as on the dielectric curing properties. In these experiments, the sample set the limit for maximum power. A substrate with better heat tolerance, is likely to shift the optimum towards shorter pulse lengths. (**Paper 4**)

Table 2.2: Energy consumed during curing process for all pulse lengths from the data in 2.7 (**Paper 4**).

Sample	current (mA)	number of pulses	Total energy (J)
1-min DC	320	1	27
100 ms	550	1	0.14
50 ms	550	10	0.68
10 ms	700	30	0.66

In conclusion, pulse heating has many advantages over DC heating, which makes it attractive for high volume production. An increased spatial temperature gradient at the edge of the line guarantees better alignment accuracy, which is also less dependent on changes in the line cross-section. Due to decreased heat dissipation into the substrate, higher temperatures can be used to cure the dielectric than is possible with DC current heating, and good alignment can be achieved on substrates with relatively high thermal conductivity. The polymer cross-linking time decreases at higher temperatures, thus decreasing the process time. With silver samples on a PET substrate, the shortest process time was achieved with one 100-ms pulse, which is only 1.7 % of the time needed for a DC current. Due to a significant decrease in process time also the total energy consumption in the process decreases significantly. The shorter the pulse, the more heating power is needed, but the decrease in time is more significant than the increase in power. (**Paper 4**)

3 Passivation of an OLED anode current distribution grid

A promising application for the Joule-heating-based self-alignment method is the passivation of OLED anode current distribution grids. The improved performance of OLEDs (Reineke et al., 2009) have made them potential candidates for flat, flexible and large-area lighting sources (Tyan, 2011). However, large-area OLEDs suffer from low conductivity of the transparent anode, which causes a lateral voltage drop across the anode and leads to inhomogeneous light emission (Neyts et al., 2006), as shown in Figure 3.1 a).

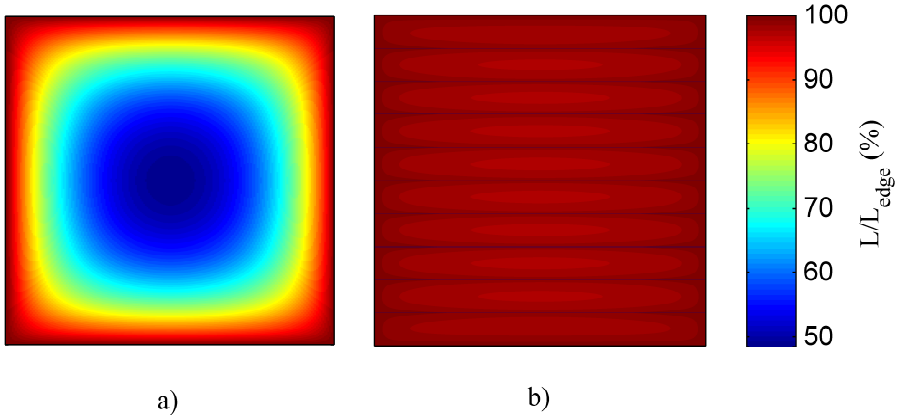

Figure 3.1: Luminance of a 10 × 10 cm^2 OLED a) without and with b) a metal grid. Adapted from **Paper 3**

Conductivity can be increased by integrating a metal grid with the transparent electrode. The grid lines, however, reduce the device active area. Therefore, thick and narrow metal lines would help maintain high conductivity while minimally reducing the device luminance area. (Slawinski et al., 2013) The effect is shown in Figure 3.1, where OLED luminance is shown without and with a metal grid.

The active layers between the electrodes are extremely thin, making the device prone to short circuits. To prevent shorting of the lines and the cathode, the metal lines must be either passivated (Choi et al., 2011), or an embedded structure must used for a flat anode surface (Galagan et al., 2011). Such a structure has been demonstrated for an organic solar cell, but the same design rules apply equally to OLEDs. Because a passivation layer further decreases the luminescent areas of the OLED, it must be accurately aligned to minimize

area loss. Printing or photolithography can be used here to align the passivation layer. As discussed in Chapter 1, printing suffers from low registration accuracy and thus requires significant over-printing, whereas photolithography is a relatively expensive process and requires an additional alignment step which is challenging in high throughput large-area production. In contrast, Joule-heating-based self-alignment offers good registration accuracy without alignment steps. Thus this chapter focuses on the feasibility of Joule heating for passivation of current distribution grids.

3.1 Optimization of grid design

When heating a grid instead of single lines, the spatial resolution of the dielectric layer depends not only on the thermal properties of the substrate and the transparent anode but also on the geometry of the grid. The spacing of the grid lines affects the locality of heating, and the grid structure affects current distribution across the grid. These design rules were studied for different grid structures with FEM modelling. Because the stationary assumption was made in the model, pulsed heating will slightly change the results presented here.

3.1.1 Current model

For an even temperature distribution in all grid lines, the current during Joule heating must be equal in all lines having the same cross-sectional area. The current was thus modelled with a 2D model of different grid types: a hexagon grid, a square grid, and a line group (Figure 3.2). The calculations were made using Ohms law with an electrical conductivity model of the AC/DC Module. Material parameters were chosen to correspond to the 3D geometry used in the thermoelectric model. (**Paper 3**)

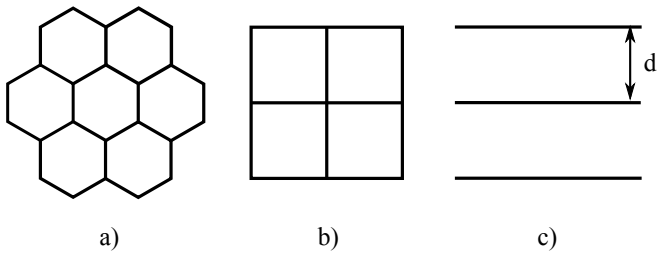

Figure 3.2: Different grid designs used in the current model: a) hexagon grid, b) square grid, and c) line group. (**Paper 3**)

To deliver power to the device, highly conductive bus-bar circulates the active area of the OLED. However, during Joule heating the bus-bar provides a low resistance path for the current, through which the current bypasses the grid itself. Thus the bus-bar or parts of it must be deposited after Joule heating. (**Paper 3**)

The hexagon and square grid required a separate pad for each grid line; furthermore, horizontal and vertical lines had to be passivated in separate runs. Of the grid designs, the square grid was the better option for Joule heating, because it provided a better current homogeneity, a 3% variation everywhere except near the pads, where it was 15%. This variation was, however, compensated for by heat conduction into the pads. In the

hexagon grid, the variation was significant, about 25% depending on the location of the line. (**Paper 3**)

The line group design provided an equal current in each line during Joule heating, making it thus the most promising design. Moreover, because the lines were electrically connected only by the bus-bar, only one heating step was required. The part of the bus-bar perpendicular to the grid lines and the grid lines can be printed in the same pass, whereas the parallel part must be printed after the Joule heating step. (**Paper 3**)

3.1.2 Thermoelectric model of a line group

During simultaneous Joule heating of all the lines in a line group, adjacent lines may affect each other's heating localization. As a result, the temperature at the border of the anode remains lower than in the centre, where the lines are surrounded by heating elements. To achieve fully passivated grid lines with an even overhang of dielectrics, the temperature should be equal in all lines. Thus the effect of the line group on temperature was modelled. The number of lines was increased until the saturation of the maximum temperature. The results were calculated for different line pitches d (see Figure 3.2).

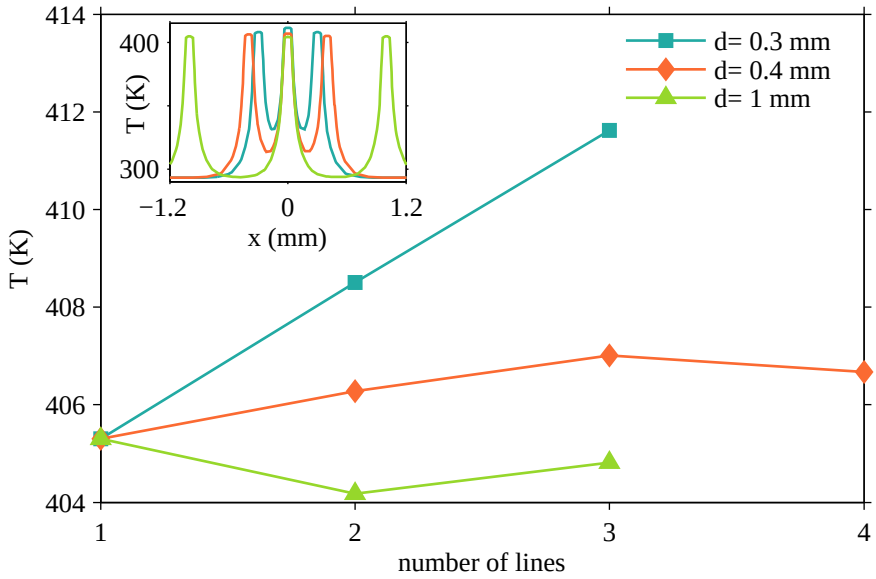

Figure 3.3: Maximum temperature in a line group on a PET substrate as a function of number of lines. (**Paper 3**)

The result for a plain PET substrate is shown in Figure 3.3. The inset shows a temperature profile for a group of three lines. When the lines were 0.3 mm apart, the central line heated the most. Therefore, for this line pitch, the thermoelectric model for individual lines does not accurately describe line groups. For line pitches 0.4 mm and 1 mm, the temperature is equal in all lines, though the number of lines has a slight effect on it. The temperature saturates already with 3 lines. In conclusion, the one-line model can be used to describe line groups, when the line pitch is 0.4 mm or more. The results can also be applied to a PEDOT:PSS-coated PET substrate, because a PEDOT:PSS layer does not decrease the selectivity of heating, as was shown in Figure 2.4. (**Paper 3**)

Because ITO decreases the selectivity of heating, simulations were repeated for the ITO-coated PET. Figure 3.4 shows that the minimum line pitch that provides homogeneous heating is higher on the ITO-coated PET than the PET substrate. With a line pitch of 0.8 mm, the temperature increases slightly as lines are added until it saturates with four lines. The inset in Figure 3.4 shows that with a line pitch of 0.8 mm, the temperature remains equal in all lines. Thus with an ITO-coated PET substrate the distance between lines should be more than 0.8 mm. (**Paper 3**)

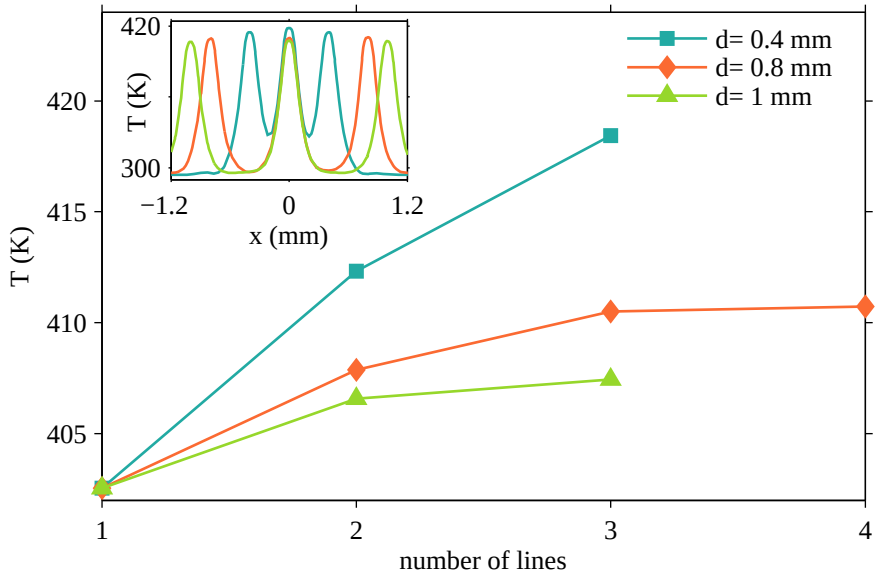

Figure 3.4: Maximum temperature in a line group on a ITO coated PET substrate as a function of number of lines. (**Paper 3**)

3.2 Passivation of evaporated lines

To show the feasibility of the process for OLED manufacturing, shadow-mask-evaporated OLED anode grid samples were passivated. ITO-coated glass (ITOGLASS 15P from VisionTek Systems Ltd.) was used as substrate. The sheet resistance of ITO was 15 Ω/□. The current distribution grid consisted of three 250-nm thick and 200-µm wide silver grid lines with a 5-mm line pitch. A spin-coated dielectric (Bectron AL14-018H from ELANTAS Beck) was cured using five 5 ms, 7.5 A current pulses. These were generated by a DC power source (Keithley 2260B) and a microcontroller platform (Arduino) driven current pulse circuit. To produce dielectric films with different thicknesses, the following samples were fabricated: a one-layer dielectric spin-coated at 2000 or 500 rpm and three layers of dielectric spin-coated at 2000 rpm. Joule heating was performed between the depositions of all the dielectric layers.

Figure 3.5 shows a microscope image of a grid line with a photograph of the current distribution grid in the inset at left. Here the passivation layer is a three-layer dielectric. Newton fringes are just visible near the bus bar and the edge of the line, indicating the end of the dielectric layer. The overhang of the dielectric was between 1 µm and 3 µm

when the line width was constant. However, at the location where the line was about 16 µm (7.5 %) narrower than elsewhere, the overhang increased to about 6 µm.

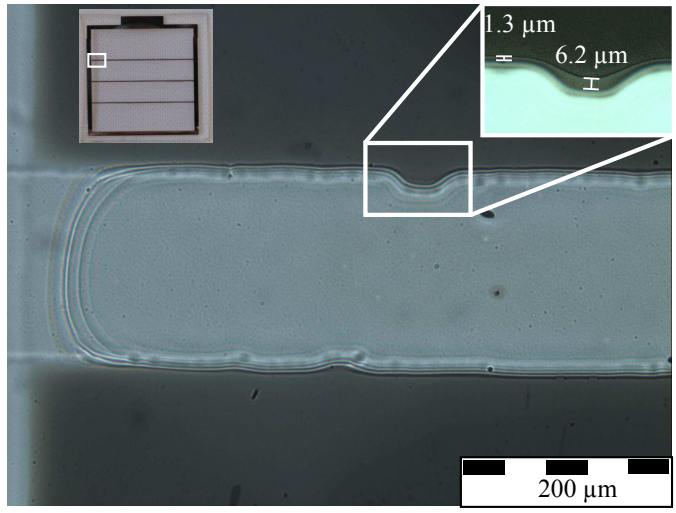

Figure 3.5: Microscope image of a passivated silver grid line on an ITO-coated glass substrate.

Dielectric film thicknesses were measured using an optical profilometer. The results are shown in Figure 3.6, where the gray bar stands for a 250 nm thick metal line. The one-layer dielectric, spin coated at 2000 rpm, was 400 nm thick. However, the film was not of even thickness: at the edge of the line high peaks are visible in the profile. The peaks result from dewetting of the dielectric during Joule heating. Because the polymer used in the experiments was fluid before it cross-linked, dewetting likely resulted from Marangoni flow induced by the surface tension gradients caused by the local heating of the grid line (Kalpathy et al., 2013). At the metal-polymer interface, the dielectric cross-linked before dewetting, but further away it dewetted, resulting in a thin dielectric layer in the middle of the line.

Dewetting was also observed in the profile of the three-layer dielectric, spin-coated at 2000 rpm, though in the layers deposited on top of the first dielectric layer it was not as strong as in the first layer. This may have been the result of two factors that can make the layers behave differently. First, the first layer is applied on ITO-metal pattern. A wettability gradient thus exist there caused by the different surface energies of the metal and ITO, whereas the second and third dielectric layers are applied on polymer on ITO substrate. The wettability of a polymer liquid on a polymer is likely better than a polymer liquid on a metal or ITO. Thus less heating is needed for a Marangoni flow to occur in the first dielectric layer than in subsequent layers. Another possible explanation is that the upper layers are further away from the heat source, resulting in a smaller spatial temperature gradient and thus also smaller surface tension gradients; consequently, the film has a longer perturbation time (Kalpathy et al., 2013). In any case, due to dewetting, a three-layer dielectric is 4.5 times thicker than a single-layer dielectric. The maximum fraction of thicknesses expected is three.

The thickness of wet film seems to affect dewetting. No dewetting pattern is visible in the profile of the single layer dielectric deposited by spin coating at 500 rpm. The thickness of the cross-linked layer is 1.2 µm, which is 0.8 µm thicker than the layer spin-coated at

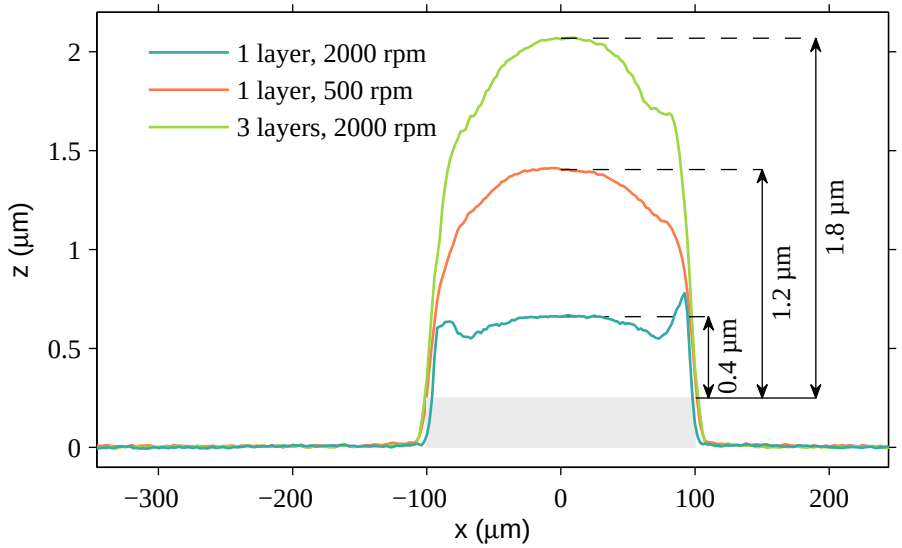

Figure 3.6: Height profiles of passivated grid lines measured with an optical profilometer for dielectric films with different thickness. The gray bar stands for a metal line.

2000 rpm. Thus the surface tension gradient for the thicker film is smaller than that for the thinner film. This cannot, however, be the only explanation, since dewetting is visible in the profile of the three-layer dielectric, which is thicker than the one-layer dielectric spin-coated at 500 rpm. The wet film may thus have been significantly thicker than the cross-linked film. In this case, dewetting could not be observed in the profile, because even if it occurred, the difference is not visible in the profile. The film may also have been thick enough for the temperature on its surface to approach ambient temperature.

Due to the ITO layer, leakage currents through the films could not be measured. All the films were, however, relatively thick, smooth, and with no visible holes. It is thus reasonable to expect negligible leakage current through the dielectric in OLED operation. To estimate leakage, measurements were conducted on a passivated silver line on PET. One dielectric layer was spin-coated at 2000 rpm, and the conductor was heated for 100 ms at 600 mA. The Joule heating parameters were selected to obtain approximately 2-µm dielectric overhang to correspond to the passivation layer on the grid. The leakage through the film at 5 V was of the order of 10^{-9} A/cm^2. Though the films on PET do not exactly compare to those on ITO-coated glass, the results predict a low leakage current during OLED operation.

3.3 Passivation of printed lines

When aiming at high volume manufacturing, the optimum approach is to print the current distribution grid. Because printed lines may vary greatly in line width within the line, patterning the passivation layer by photolithography would require a large dielectric overhang and offer no significant advantage in registration accuracy over printing. The accuracy of the Joule heating process is less prone to changes in line geometry than other passivation methods, while being cost-effective. Thus Joule heating is a very attractive method to passivate printed current distribution grid. For these experiments

current distribution grids were screen printed at the TNO/Holst centre. The grid lines were passivated at TUT and sent to Philips GmbH Innovative Technologies for OLED deposition.

The substrate in the experiments was ITO-coated glass. The sheet resistance of the ITO film was 10 $\Omega/\square$. A silver current distribution grid was screen printed on the ITO leading to a sheet resistance of 0.6 $\Omega/\square$ of the grid. The typical thickness of the printed silver grid lines were 3 µm with a width of 90 µm, and a line spacing of 2 mm. The total active area of the device was about 900 mm^2 in size. (For more details see Supporting information of **Paper 4**)

Six 75-ms, 13-A current pulses were used to cure the dielectric. The power source setup was the same that was used to passivate evaporated grid lines, except that instead of one power source, two sources were connected in series to provide the required output voltage. Thus in these two experiments, the pulse profiles were not comparable. Since the surface properties of printed silver lines differ from those of evaporated lines, dewetting the dielectric took place with dielectric layers that were not extremely thick. To obtain films thick enough for dewetting not to occur, a highly viscous solution of dielectric (Bectron AL14-028 C) and Propylene glycol monomethyl ether acetate (PGMEA) was mixed. In the solution, the dielectric to PGMEA volume ratio was 1:4, and the dielectric was drop-coated on the current distribution grid. (**Paper 4**)

Figure 3.7 shows microscope images of a passivated grid line. The grid lines were fully passivated with excellent alignment accuracy; the dielectric overhang was less than 5 µm, though the line width varied from 80 µm to 100 µm, a considerably large variation. (**Paper 4**)

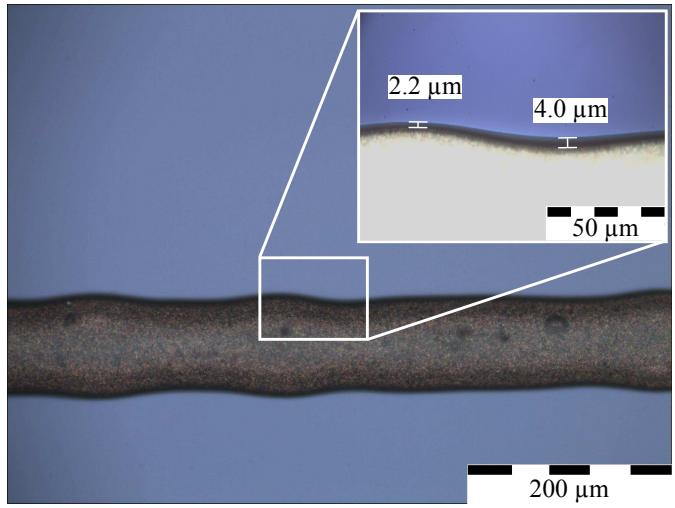

Figure 3.7: Microscope images of a passivated printed silver line. Adapted from **Paper 4**.

There was no significant difference in the alignment accuracy of the passivation layer between the shadow-mask-evaporated and printed lines. The printed lines had more long-scale variation in the line cross-section than the evaporated line, but as discussed earlier, the shape of printed lines increases the selectivity of heating (**Paper 3**). Thus the overhang is not greatly enlarged by the changes in the line cross-sectional area. Furthermore, the film thickness of drop coated dielectric varied greatly without a noticeable effect on

dielectric overhang. Thus it can be concluded that dielectric coating method is not critical for the process.

To demonstrate an OLED device, a phosphorescent white small molecule organic multilayer stack was evaporated on ITO/glass substrate (reference sample) and on ITO/glass with passivated current distribution grid. The cathode electrode was a 100 nm thick Al layer. Prior to OLED deposition, the substrate was cleaned by rinsing, brushing, and ultrasonic bath. After cleaning, samples were annealed 1 h at 120 °C in inert atmosphere to remove residual water from the dielectric. The passivation layer protected the grid lines from the cleaning procedure. Though the adhesion of the printed silver lines was good, they could not withstand the cleaning conditions without the passivation layer. A more detailed explanation of the OLED manufacturing is presented in Supporting information of **Paper 4**.

The resulting photographs of the OLEDs and the IV-curves are presented in Figure 3.8. The blurred black artefacts at the vicinity of the grid lines shown in Figure 3.8 b) are due to water outgassing from the polymer. The annealing did not completely remove water contaminants from the passivation layer. To reduce the artefacts more a hydrophobic polymer should be used.

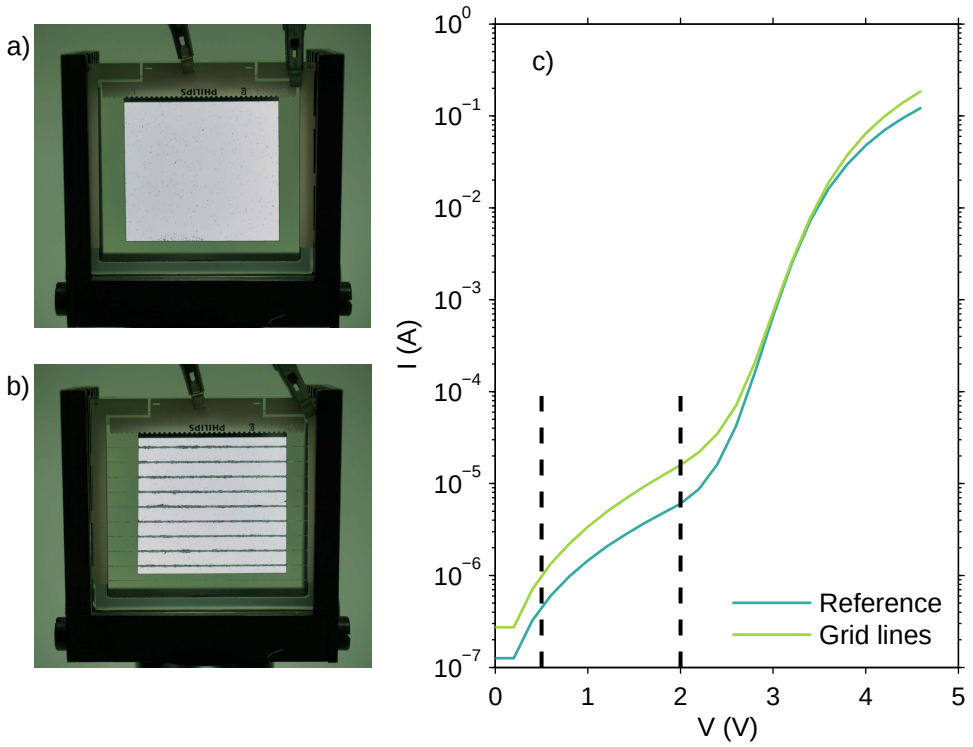

Figure 3.8: Photographs of a) a reference OLED and b) an OLED with current distribution grid lines during operation. c) IV-curves of the OLEDs. Adapted from **Paper 4**.

The IV-curves for the reference OLED without the grid lines and the Joule heating passivated OLED are presented in Figure 3.8 c). The dashed lines highlight the non-emitting voltage range from 0.5 V to 2 V. The leakage current for the device with grid lines is the same order of magnitude as for the reference device. The grid lines increase slightly

the forward current. Thus it can be concluded from the results that the surface topology of the printed lines allow reliable OLED operation, and the Joule heated passivation layer offers good enough insulation of grid lines.

In this chapter the Joule heating method was reviewed from the point of view of a cost-effective tool for passivation of OLED anode. The process places design criteria for the grid line design and line spacing. However, the preferred design, a line group, is simple to manufacture. One remarkable advantage of the Joule heating is the compatibility of the process with economically feasible screen printed grid lines. Though the variation of the cross-sectional area of the printed lines is significant, it does not markedly increase the dielectric overhang. In fact, the overhang was of the same order of magnitude with printed lines as with shadow-mask-evaporated lines. Thus it can be concluded that the Joule heating based passivation process has potential for low cost manufacturing.

4 Electrode patterning using microcutting

This chapter deals with the microcutting of metal electrodes on a polymer film. Both nanoimprint lithography (NIL) and microcutting can be used for this purpose, and they are well suited for large scale production. Whereas NIL is used to replace optical lithography and requires multiple process steps, including resist application and etching, microcutting is a direct patterning method and requires no chemicals. In microcutting, a stamp is pressed into contact with the substrate, and pressure is used to deform the substrate. Microcutting can be performed at room temperature or at elevated temperatures. The former method is defined here as microcutting with the NIL-tool and the latter microcutting by hot embossing. Whereas the NIL requires multiple process steps (pattern imprint, etching and resist removal), microcutting with the NIL-tool uses the stamp to directly cut the electrodes. In this work NIL-tool was only used to imprint the microcut, and thus etching and resist removal was not needed.

NIL is a widely used and promising high resolution and high throughput patterning technology, which allows fabrication of a variety of devices, for example, for electrical and optical applications (Guo, 2004). One electrical application is the organic field-effect transistor (OFET) (Cheng et al., 2006; Rothländer et al., 2011).

By optimizing the NIL process, feature size can be reduced down to 20 nm (Viheriälä et al., 2007). In addition, Ahn and Guo (2009) showed that by using flexible moulds instead of conventional stamps NIL technology can be transferred to a continuous roll-to-roll imprinting for high-speed, large-area nanoscale patterning. When the aim is small feature size, patterning of silicon is easier to control than patterning of metal; thus silicon templates with inverted polarity can be replicated on nickel plates, which are compatible with roll-to-roll manufacturing (Guo, 2007; Haatainen et al., 2006).

Though direct microcutting cannot achieve the same resolution microcut as NIL, wide metal lines down to 100 nm width can be patterned with microcutting by hot embossing (Stutzmann et al., 2000a). Sub-micrometer ceramic and conducting polymer features have also been successively microcut on a polymer substrate (Stutzmann et al., 2000a, 2002). Moreover, a vertical-channel OFET was demonstrated with this technique (Stutzmann et al., 2003).

One challenge in roll-to-roll production of electronic products is accurate alignment and patterning of microscale structures. Such a challenge can be overcome by combining fast low resolution patterning with roll-to-roll fine resolution microcutting. For example, rough patterning by shadow mask evaporation can be followed by NIL microcutting to define final microelectrodes.

This chapter introduces a fabrication method suitable, for example, for a thin film transistor (TFT). The method combines coarse patterning followed by microcutting. Narrow electrodes defined by microcutting were passivated by Joule heating (**Paper 1**). In addition to study of the stamp geometries, microcutting by hot embossing and with NIL-tool are compared.

4.1 Method

Figure 4.2 a) shows the topography of the stamp used for microcutting. The separation between the microblades was 10, 30, 50, 70, or 150 µm. Three different sets of stamps were fabricated using different processes. The first set was wet-etched, the second RIE-etched, and the third fabricated by wet-etching followed by thermal oxidation and oxide removal. Figure 4.1 shows scanning electrode microscope (SEM) images of the stamps. The inset in the figure illustrates the structure of the microblades and the location of the cross-section (Figure 4.1 a)) and the top view (Figure 4.1 b)). For more details, see **Paper 5**. The different stamp sets were designed to improve the yield of microcutting.

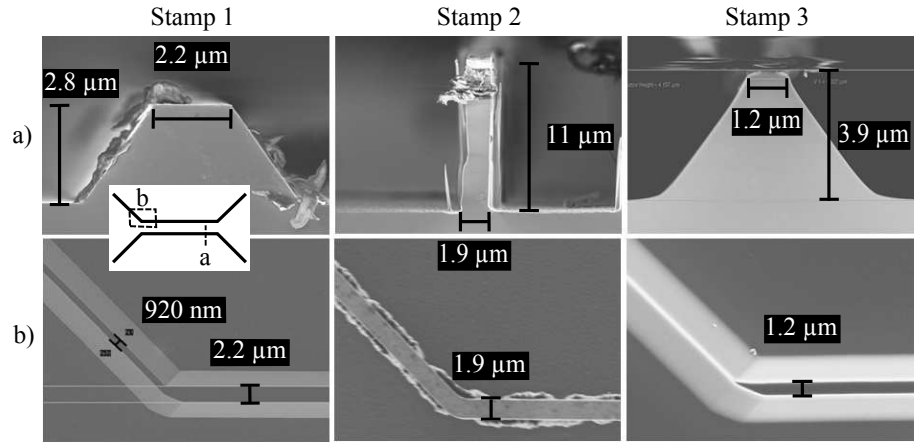

Figure 4.1: SEM-images of the stamps used in the experiments. a) Cross-section and b) top view of the cutting blades. Inset: schematics of the stamp. (**Paper 5**).

The patterning process is shown in Figure 4.2 b). Large cross-shaped electrodes were pattered on a PET substrate by shadow mask evaporation. To define the final fine resolution electrode pattern, a stamp was pressed into contact with the substrate (Figure 4.2 b) steps 1-2)). Subsequently, the load was removed, and the initial electrode was separated into three high resolution electrodes (Figure 4.2 b) step 3)). Finally, a dielectric was applied to the substrate and aligned on electrode 2 by Joule heating (**Paper 1**) (Figure 4.2 b) 4). This structure could be used, for example, as a transistor platform, where electrode 2 is the gate, electrodes 1 and 3 are source and drain, and the cured dielectric is a self-aligned gate dielectric.

To obtain a transistor a semiconductor layer need to be printed across the insulated gate electrode from the source to the drain. In this structure the length of the semiconductor edge parallel to the gate electrode defines the transistor's channel width, whereas the channel length is defined by the gate electrode width and the overhang of the dielectric layer. Thus the accurate alignment of the dielectric layer is essential for the device

performance. In Chapter 3, 2 µm overhang on ITO coated glass was demonstrated. In microcut substrate this size of overhang would fill the cutting trace, and thus it is not expected to have large effect in the transistor behaviour. Though the thermal properties of the metal coated PET substrate differs significantly from those of ITO/glass.

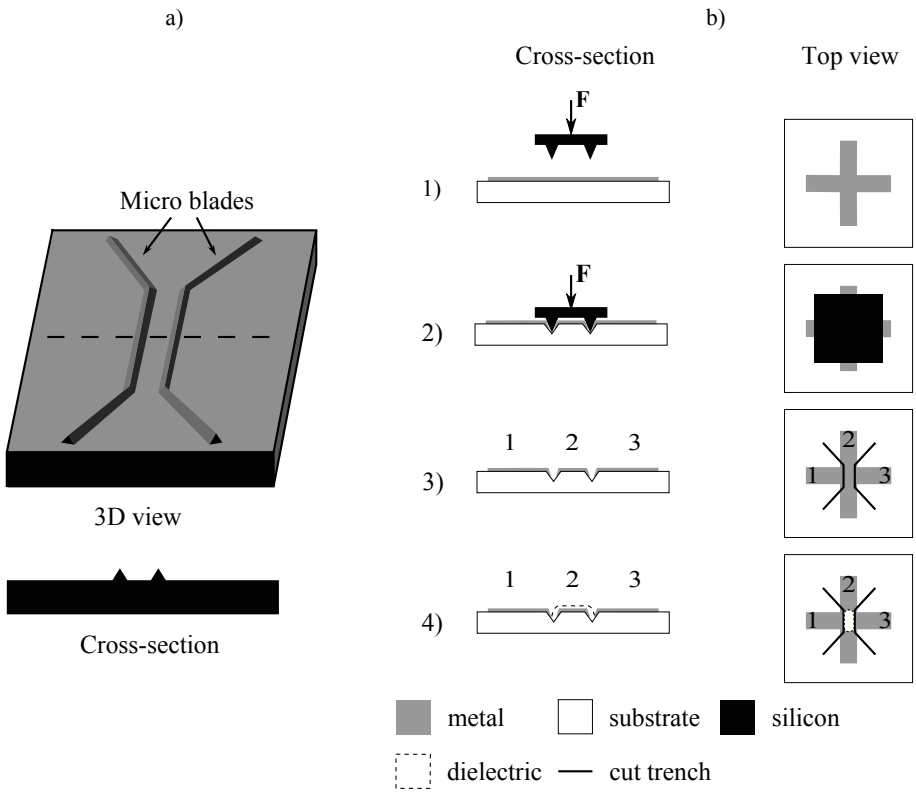

Figure 4.2: a) Stamp topography. b) The method to fabricate a thin film transistor platform. Left column, cross-section view; right column, top view. 1-2) A cross-shaped electrode is pressed with a silicon stamp 3) separating three electrodes. 4) Joule heating is used to pattern a dielectric layer on the narrow electrode. Note that the separation between the blades and the electrode pattern is not to scale; the width of the electrode is between 7 and 100 times the blade separation width. Thus low resolution alignment can be used during stamping. Adapted from **Paper 5**.

The initial cross-shaped electrode was 1 mm in line width and 50 nm in metal thickness, whereas the separation between the micro blades was from one to two orders of magnitude smaller than the width of the initial electrode. Since the low-resolution electrode pattern was large compared to the high-resolution micro blade pattern, alignment of the stamp was not critical.

Microcutting was performed both by hot embossing and with the NIL-tool to compare the methods, which are both described in the following sections.

4.2 Microcutting by hot embossing

Microcutting by hot embossing is affected by several factors, which are described in this section. The process temperature depends on the properties of the polymer substrate in that the polymer is in its solid state. Because a substrate in a liquid phase during microcutting would only result in bending and deep-drawing of the metal layer, embossing should be done with a substrate in a plastically deformable solid state. Polymer flow should take place only after the metal is pierced. For a semi-crystalline polymer, the optimal embossing temperature is between its glass transition temperature and its melting point, whereas with amorphous polymers, embossing should be performed at around the polymer's glass transition temperature. (Stutzmann et al., 2000a) The substrate used in the experiments reported here was PET (Melinex ST506 from DuPont Teijin Films), a semi-crystalline polymer with a glass transition temperature of 78°C and a melting point of 255°C.

At elevated temperature, the polymer is ductile and does not undergo fracture as easily upon impact as at temperatures below glass transition. (Callister, 2007, p.524-526) Thus the polymer can be processed in its solid state without fracture. The polymer flow depends on its viscosity, and because the viscosity is high close to the polymer's glass transition temperature, embossing is slow. (Scheer and Schulz, 2001) With semi-crystal polymers, one should take into account that the shrinkage of the polymer upon crystallization may cause it to deform after the load is removed. The polymer must hence be cooled below its glass transition temperature to allow crystallization to take place before removing the stamp. (Stutzmann et al., 2000b)

Hot embossing experiments were run with stamp 1 (Figure 4.1) on shadow-mask-evaporated copper electrodes on a PET substrate. The stamp was of height 2.8 µm and the tip of the blade was of width 2.2 µm in its parallel part and 0.92 µm in its diagonal part. The width of the blade tip together with the force of the stamp pressed on the substrate define the pressure at the substrate. When the pressure is sufficient, the plastic substrate deforms, stressing the thin metal layer evaporated on the substrate. When the pressure is sufficient, the metal is stressed over its fracture point and it breaks. The strain durability of the metal, however, depends on the thickness of the film. For a 60-nm thick gold film, the strain durability is 1 % (Neugebauer, 1960). This value can only be used as an estimate, because then it depends on the material, deposition method, and the width of the film. The maximum strain that stamp 1 could create was, however, 60%, which, in fact, was significantly higher than the strain durability of a thin gold film. Therefore, with this stamp the limiting factor was the pressure defined by the width of the blade tip. This width could not be decreased by deeper etching, because the reduction in line width of diagonal lines was faster than that in parallel lines. Thus the reduction in line width of diagonal lines set the limit to the etching depth and thus to the tip width of the parallel lines as well. (**Paper 5**)

In the hot embossing experiments, a force of 3 kN was applied to the substrate with a manual press (Rondol 10 Tonnes Bench Hand Press) for 60 minutes to separate the electrodes. Substrate and stamp temperatures were elevated to 115 °C, which exceeded the substrate's glass transition temperature but remained below its melting point. After embossing, the temperature was decreased below the glass transition temperature to 70 °C. Finally, the load was removed. (**Paper 5**)

The time needed to ensure sufficient microcutting was relatively long, because the polymer material was heated only slightly above its glass transition temperature, which slowed

down the flow of the polymer. To decrease the process time, either the embossing force or the temperature should have been increased. However, the blade of stamp 1 was sufficiently blunt, and the required force would have broken the fragile stamps. Because adhesion of copper to the substrate was not sufficient, a thin copper layer adhered to the stamp during hot embossing, as seen in Figure 4.3, which shows microscope images of the hot embossed electrodes that are slightly translucent. If the process temperature had been increased, more copper would have adhered to the stamp. In addition, heating fully oxidized the copper at the narrow electrode, which is the most critical element of this architecture for successful Joule heating. Thus oxidation further limited the embossing time. (**Paper 5**)

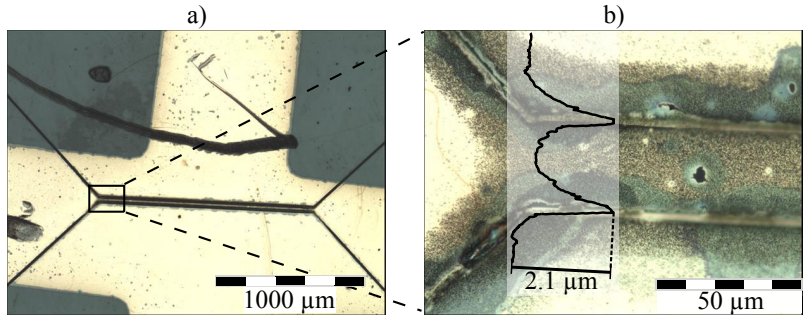

Figure 4.3: Copper electrodes on PET hot embossed with Stamp 1. Microscope images with magnification of a) 5× and b) 100× with a profile of the microcut imaged with optical profilometer. Adapted from **Paper 5**.

The profile of an embossed microcut measured with an optical profilometer (Veeco Wyko NT1100) is shown in the inset of Figure 4.3 b). The height of the structure is 2.1 µm, which is 75 % of the blade height of the stamp. Furthermore, the profile between the microcuts is rounded from the profile of the stamps. A complete transfer of a relief structure can be challenging, because the flow of the polymer substrate is hindered in the solid state. On the other hand, the substrate is coated with a metal layer, which restrains the polymer flow. Embossing has increased the surface roughness of the microcut electrode, probably because of the poor adhesion of the metal to the PET substrate. (**Paper 5**)

The yield of successful microcutting was 50%. The leakage current between the separated electrodes was less than 1 nA at 15 V. (**Paper 5**) A low leakage current between electrodes is not the only microcutting requirement. When Joule heating is used in combination with microcutting, quality requirements are imposed on the narrow electrode. An unevenly oxidized conductor behaves like a geometrically uneven conductor. Selecting gold as electrode material overcomes this oxidation issue. However, its adhesion to the substrate must still be improved to prevent transfer of the metal to the stamp.

4.3 Microcutting with a NIL-tool

The main difference between microcutting by hot embossing and microcutting with a NIL-tool is that the latter is done in a brittle state of the PET substrate. The polymer is fractured with a short impact, whereas hot embossing is done slowly with the polymer

in a ductile state. At room temperature, the ductile-brittle transition of PET occurs at 40% elongation (Chapleau and Huneault, 2003). The process is fast, because it is not necessary to wait for the polymer to flow in its solid state, though after the load is removed, some deformation returns through elastic strain recovery. (Yao and Nagarajan, 2004) Due to the fracture and strain recovery of the polymer, microcutting does not accurately reproduce the microstructure of the stamp. In the application here, however, accurate reproducibility of the master was not intended; only separation of the electrodes was aimed at.

Microcutting experiments with a NIL-tool were repeated with all stamp designs and gap sizes. The metal electrodes were separated with a mask aligner (EVG620, EV-Group). The stamp was pressed into the substrate at a force of 1.7 to 1.8 kN, depending on the blade and pattern design. In contrast to the hot embossing experiments described earlier, microcutting was carried out at room temperature. The load was applied only for 10 s. (**Paper 5**)

Figure 4.4 shows microscope images and corresponding profiles of the microcuts. Because the separation between the microblades had no significant effect on microcutting, only results obtained with stamps of 30-µm separation between the blades are presented. The first column shows the microcut patterned with stamp 1. The resulting microcut is significantly shallower than the hot embossed pattern: in height the structure is only 0.5 µm (Figure 4.4 b)). However, the force applied to the stamp was only 60 % of that used in the hot embossing experiments. Furthermore, some degree of recovery was expected after the load was removed, when a ductile material is stressed beyond the threshold of plastic deformation. (Yao and Nagarajan, 2004) In hot embossing, deformation is irreversible, because the polymer hardens before the load is removed. The yield of microcutting with the NIL tool was low with stamp 1. Incomplete separation localized mostly in the diagonal part of the stamp. (**Paper 5**)

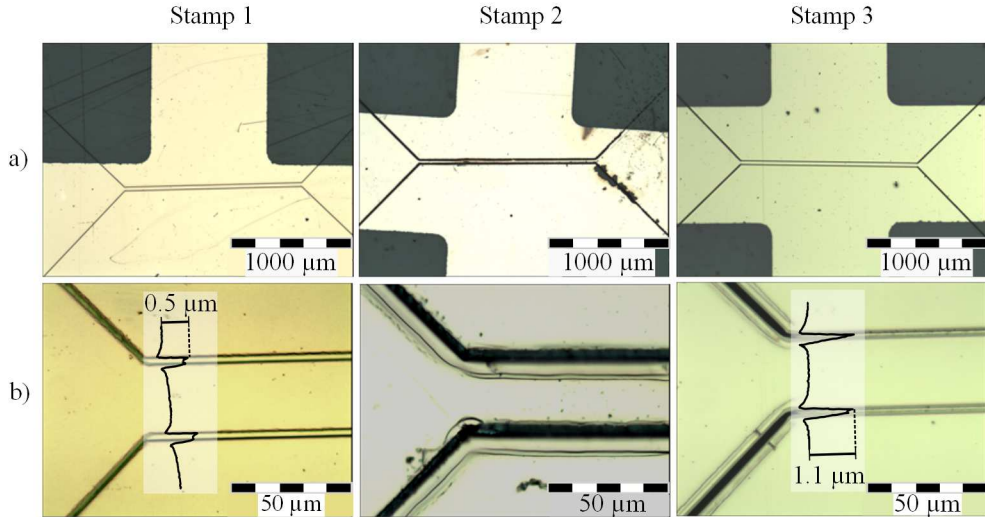

Figure 4.4: Copper electrodes microcut with stamps 1 and 2 and a gold electrode microcut with stamp 3. Microscope images of the electrodes with a)5× and b) 100× magnification with a profile of the microcut imaged with an optical profilometer. Figure from **Paper 5**.

A new set of stamps was designed to increase the aspect ratio of the microblade and

the yield of the microcutting process. The blades of stamp 2 design were defined by anisotropic RIE-etching, and the resulting height and width of the tip were 11 µm and 1.9 µm, respectively (Figure 4.1 b)). The blade dimensions were sufficient to bring the metal to tensile strength. Etching, however, was not fully successful as some burr remained near the edges of the blade. The burr increased the contact area between the tip and the substrate, decreasing the local pressure during microcutting. (**Paper 5**)

The second column of Figure 4.4 shows microscope images of copper electrodes patterned using stamp 2 and the NIL-tool. A profile of the microcut could not be obtained with an optical profilometer, but its height was measured as 9 µm by using SEM (Figure 4.5). The image shows clearly that the polymer had fractured during the process. The microscope and SEM images prove that stamp 2 produced the deepest and also the widest relief structure. In addition to blade width, the depth of the stamp pressed into the substrate also defines the width of the relief structure. Because the microcutting experiments were made with different stamps, and because the stamps of design 2 varied widely in quality, the yield of the microcutting process could not be determined. However, Figure 4.4 makes it obvious that of all the experiments the microcut produced with stamp 2 is the lowest in quality.

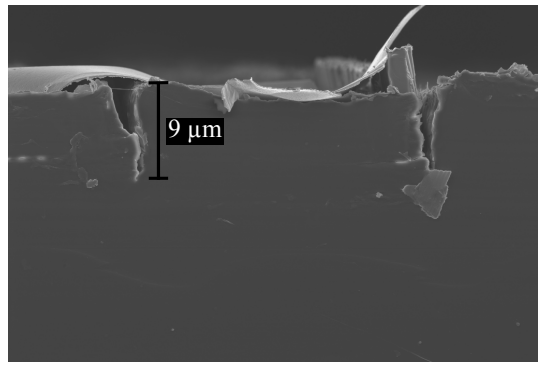

Figure 4.5: A SEM image of the cross-section profile of a microcut sample using the NIL-tool and stamp 2. Adapted from the supplementary data in (**Paper 5**).

Figure 4.4 shows that the best results were obtained using stamp 3 and the NIL tool. To retain the quality but to improve the geometry of stamp 1, it was developed further by thermal oxidation. The resultant blade structure of stamp 3 design was higher and narrower than that of stamp 1 design. The final blade height was 3.9 µm, and the parallel blade tips were 1.2 µm wide, whereas the width at the diagonal part was only tens of nanometres (Figure 4.1).

The depth of the microcut produced with stamp 3 was 1.1 µm, and the cut is clean (Figure 4.4). The yield of the process was 100 %, if the outlines of the stamp were free of burr. The leakage current between the electrodes was only of the order of tens of picoamperes at 15 V.

In the application presented here, the substrate did not need to precisely conform to the shape of the stamp. The most important parameters were leakage between the electrodes when voltage was applied to the device, surface roughness, and separation between the microcuts. The patterns fabricated by hot embossing conformed to the geometry of the blade better than the microcuts created with the NIL-tool. Moreover, the yield of the hot embossing process depended less on stamp geometry than on microcutting with the NIL

tool. However, the hot embossing process had the disadvantages of high electrode surface roughness and long process time, which exceeded 1 h. In contrast, microcutting with the NIL tool produced clean and smooth electrode patterns in as short a time as 10 s.

The quality of the electrodes patterned with the NIL-tool using stamp 3 was high enough to align a dielectric layer on the narrow electrode by Joule heating with a DC current. The resultant TFT platform is shown in 4.6. The electrodes used in the experiments were gold, and the dielectric was 3 layers of poly (4-vinylphenol) (PVP) cross-linked with suberoyl chloride (SC) (for more details, see **Paper 1** and **Paper 5**).

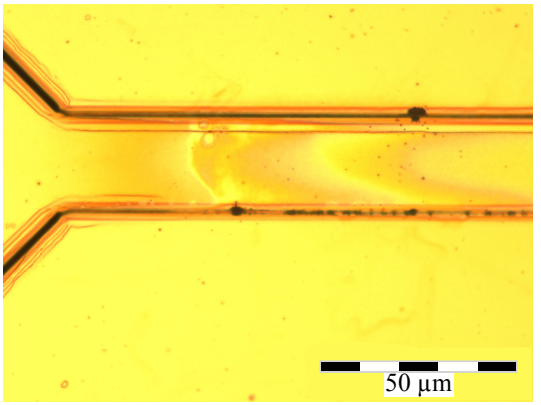

Figure 4.6: A 30-µm wide electrode passivated by Joule heating. (**Paper 5**).

The demonstration of a TFT was not successful due to peeling of the electrodes during the testing of the device. The peeling off occurred at high voltages, which are needed to switch on organic transistors. No clear reason for the peeling could not be found. Thus it would be interesting to study further if the charge transport through the metal-substrate interface could have induced an electric double layer and repulsive forces that exceeded the adhesion forces of the film. The effect of the electric double layer in the adhesion has been studied earlier. In that study, however, the metal film was not charged, and thus the double layer improved the adhesion.(von Harrach and Chapman, 1972)

The microcutting released small sections of the metal near the metal cut. At these sections the peeling started, and as the separating force is concentrated on a line rather than on surface, smaller force is needed to remove the metal. In any case the adhesion of the metal should be significantly improved to demonstrate the transistor.

The main outcome of this chapter is that high-resolution patterns can be generated by combining low-resolution patterning with roll-to-roll, scalable, high resolution microcutting. The resultant micro-electrodes can be passivated by self-alignment. The proposed method can be integrated with existing mass manufacturing methods.

5 Summary

This theses examined two alternative fabrication methods suitable for roll-to-roll manufacturing. The first method – Joule-heating-based self-alignment for dielectric patters – takes advantage of an electric current that heats a conductor locally and cross-links the polymer precisely at the location of the conductor. In the second method, a patterned silicon stamp is used to separate narrow adjacently aligned electrodes from the original rough electrode pattern. By combining these two methods a new type planar transistor platform was demonstrated.

Chapter 4 studied microcutting as a possibility to pattern metal electrode structures on a plastic substrate. This idea is not new, for Stutzmann et al. (2000a) first used hot embossing in polymer solid state to pattern optical gratings. In the present thesis, two microcutting methods were compared: hot embossing between polymer glass transition temperature and melting point and microcutting with a NIL-tool at room temperature. The latter proved the more suitable method to separate the electrodes, which was the aim of this work. The processing time with the NIL-tool was only 10 s, whereas that needed for hot embossing was more than an hour. Moreover, the microcut created by using the NIL-tool was of better quality than the hot embossed electrodes, which suffered from high surface roughness originating from unsatisfactory adhesion between metal and substrate. Consequently, microcutting with the NIL-tool has more potential for up-scaling to roll-to-roll manufacturing than the hot embossing method. The main limiting factor for successful microcutting was, however, the geometry of the stamp.

The microcut structure formed a TFT-platform, on which planar electrodes formed source, gate, and drain electrodes. The middle electrode was passivated by Joule heating to form a gate dielectric. Thus Chapter 4 shows that high-resolution patterns can be generated by combining low-resolution patterning with roll-to-roll scalable high resolution microcutting. Because of the design dimensions of the stamp and the initial rough electrode, no accurate alignment steps were necessary. The resultant micro-electrodes can be passivated by Joule heating. The proposed method can be integrated with existing mass manufacturing methods.

The Joule-heating-based passivation method was first demonstrated for single lines on a PET substrate using constant current heating. The method was initially designed to pattern dielectric onto the microcut electrodes described above, but it was later developed into a processing technique for OLED anode passivation. Because it is more complicated to passivate a grid than a single line, FEM simulation was conducted to solve design rules for the grid geometry and to establish a theoretical basis for registration accuracy.

According to simulations the line group design is the best option for a current distribution grid, because in that design the Joule heating current is equal in all lines heated simultaneously. The main factor defining the registration accuracy (size of the dielectric overhang)

is heat conduction in the substrate. By choosing a substrate material with low thermal conductivity, it is possible to limit heat conduction in the substrate. However, in some cases such a choice cannot be made. Simulations showed that a more effective way to decrease the area of heat propagation is to use short current pulses instead of a constant current. This result was also verified experimentally. With this method, an accuracy of about 2 µm was shown for the dielectric overhang on shadow-mask-evaporated silver lines on glass. The significance of the result is highlighted in Figure 5.1, which shows registration accuracies for different printing processes and roll-to-roll photolithography together with the Joule heating result. The black line stands for the target line and the grey bars for patterned layers. The process registration accuracy defines the width of the line. The figure makes it evident that with printing methods the line width necessary to cover the target line would require significant overprinting. In contrast, in registration accuracy, Joule heating is comparable to roll-to-roll photolithography.

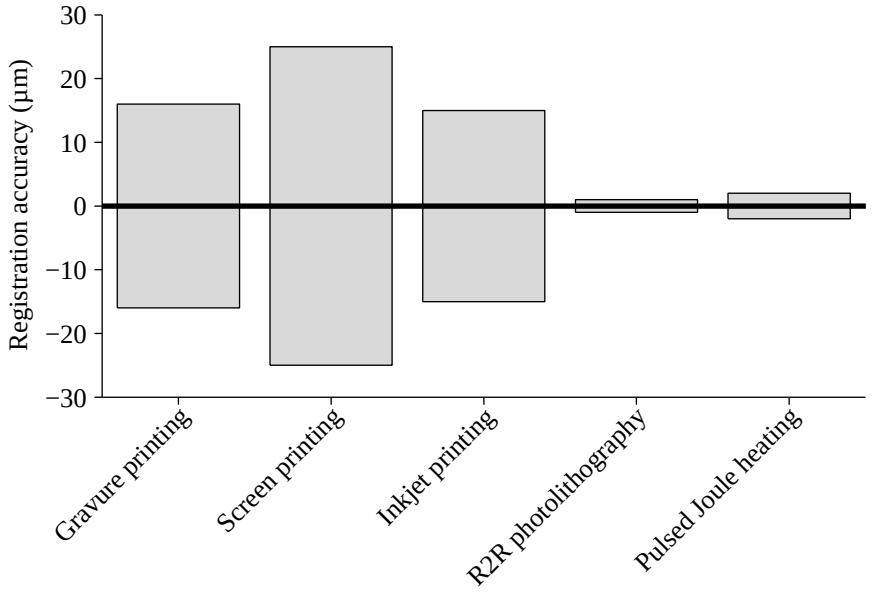

Figure 5.1: The size of the overhang needed to accurately cover the target line (black) for different fabrication processes.

Roll-to-roll photolithography is an effective method only when the target pattern is accurately defined. In contrast, the accuracy of the Joule heating process does not significantly decrease even when the target line is a printed line with large variation in its cross-sectional area. Here though the topography of the line has a positive effect on the alignment accuracy.

This thesis showed passivation of screen printed OLED anode grid lines with a typical dielectric overhang of 4 µm. The anode was implemented in an OLED device, demonstrating potential scalability of Joule heating while maintaining an excellent registration accuracy.

Pulsed Joule heating offered significant improvements in process time and registration

accuracy over constant current heating. This development has opened up a path to new research, which may be one of the enabling techniques of very low cost large-area electronics. The next interesting demonstration would be flexible OLEDs passivated by Joule heating. The grid design rules should also be reconsidered, since the accuracy of pulsed heating is less dependent than DC heating on geometrical variation in lines. Consequently, grid structures more complex than a line group should be possible to passivate.

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Publications

Publication I

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Short communication

Self-alignment method for solution-processable dielectric structures via joule heating

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ABSTRACT

We present a versatile method to create self-aligned patterns of polymer dielectric on metal by the use of Joule heating. In contrast to global thermal or light based curing, the method self-aligns the dielectric to a metal pattern on the substrate. A current-induced temperature rise along a metal line cures the insulator locally; uncured material is then removed by rinsing with solvent. We have obtained very promising results for aligning thermally cross-linkable and selectively baked dielectrics. Alignment of cross-linkable polymers is less sensitive to the rinsing step than selectively baked dielectrics. Finite-element simulations were used to determine the range of suitable curing current. After optimization of the curing parameters high yield and low leakage dielectrics were obtained.

1. Introduction

Printed electronics is being studied intensively as a promising alternative to conventional electronics, especially for inherently large-area applications or integration of multiple functionalities. Whereas conventional electronics has minimized the cost of devices by miniaturization, printed electronics can produce large area patterns at very low cost [1].

A variety of semiconducting, conducting and insulating materials is needed to print an electronic circuit; in this paper we focus on insulators, though the same concepts may be extendable to semiconductors. High quality dielectric materials are essential for electronics applications: in particular high capacitance and low leakage current are required from the transistor gate dielectric. To fulfill the needs of printed electronics, insulators should be compatible with flexible substrates and low-cost manufacturing methods. Insulating polymers can be processed as solvent based inks which enable their use in printing and coating processes. To guarantee pinhole free insulator layers, polymer films usually need to be relatively thick (a few hundred nanometers). If multiple process stages are used to manufacture a circuit, the insulator should be insoluble in solvents used in the subsequent processing steps.

Inorganic insulators usually have higher dielectric constants than organic dielectrics [2] and are insoluble in organic solvents. However, they usually require vacuum or vapor phase processes such as Physical Vapor Deposition, sputtering, Chemical Vapor Deposition or Atomic Layer Deposition. In addition, the patterning of inorganic layers by low-cost methods is also frequently challenging. Furthermore, there is some evidence that high-k dielectrics are not always the preferred choice for applications in printed electronics [3]. Therefore, there is a need for both high and low k dielectrics in printed electronics.

One approach to fabrication of inorganic insulators is electrochemical anodization of metal. Anodization is compatible with the demands of printed electronics. It is a cheap, solution based technique, and compatible with plastic substrates. Anodization has been used to create thin high quality metal oxides from aluminum, titanium, and tantalum. These metal oxides tend to have high dielectric constant and they have been used in thin-film transistor gate dielectrics, where the gate dielectric and gate electrode are automatically self-aligned [4–6].

We report here an approach that allows self-aligned patterning of solvent based, low dielectric constant organic dielectrics on metal lines. Metal lines patterned onto a substrate are heated with electric current. Localized heating cures the insulator surrounding the heated part of the line. If the insulator is cross-linkable, it is resistant to organic solvents and uncured dielectric can be rinsed away. This method has high potential in printable electronics. Whereas in electrochemical anodization process the whole metal is covered with the oxide film, here the electrode can be selectively covered with polymer dielectric layer using appropriate electrode design. For instance, it provides insulator-free areas for electrical contacts while allowing bridges for signal lines — no vias are needed. Previously, use of Joule heating was reported for selective ablation of polymer layer on a silicon nanowire [7]. In contrast to this work, we use Joule heating for the stabilization and patterning of the polymer.

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We have demonstrated self-aligned patterning of insulating polymers by selective baking in the case of poly(methyl methacrylate) (PMMA) and by thermal cross-linking in the case of poly (4-vinylphenol) (PVP) using suberoyl chloride (SC) as a cross-linking agent. Thermal modeling has been used to estimate the effect of current density on the temperature increase at the conductor.

2. Materials and methods

All the materials were purchased from Sigma-Aldrich unless otherwise noted. PMMA (weight-average molecular weight $M_w = 120{,}000$ g/mol) was dissolved in a 1:1 by weight mixture of toluene and ethyl acetate. Three different PMMA solutions where the PMMA weight percentage was 5 wt.%, 9 wt.% and 15 wt.% were formulated. The baking time of PMMA was varied between 40 to 70 min and current density was $7.8–8.5 \times 10^9$ A/m^2.

The solution of PVP/SC was formulated in propylene glycol monomethyl ether acetate (PGMEA). The PVP (weight-average molecular weight $M_w = 25{,}000$ g/mol) to cross-linker molar ratio was 10 and the PVP concentration was 50 mg/ml. Joule heating was applied with current density from 7.3 to 9.2×10^9 A/m^2, and curing time was 5 min.

A 125 μm thick heat stabilized poly(ethylene terephthalate) (PET, Melinex® ST506 from DuPont Teijin Films) film, was used as the substrate. Copper conductors of a thickness of 100 nm, width of 390 μm, and length of 5 mm were deposited onto the substrate using electron beam evaporation and a shadow mask. The polymer layer was applied to the substrate by spin coating with rate of 2000 rpm or 500 rpm. An electrical current was passed through the conductor causing heating of the narrow parts of the conductor. Due to the temperature rise at the conductor, the dielectric is cured locally above the conductor. The noncured soluble insulator can be rinsed away with the solvent as shown in Fig. 1. In the case of multiple dielectric layers, insulators were cleaned after the spin coating and curing steps.

The Joule heating was carried out with 390 μm wide copper traces. To control the heating process, a steel plate was placed under the PET substrate. Effects of the curing time and current density on cross-linking of PVP were studied. Capacitances, leakage currents, and surface roughness of the insulators were measured from devices consisting of a sandwich electrode structure.

The top electrode was evaporated on cured insulator film forming a capacitor with an area of 0.15 mm^2. Capacitances were measured with a network analyzer (Hewlett Packard 8752 A) and leakage current with a semiconductor parameter analyzer (Agilent 4155B). Breakdown voltages were investigates with a source meter (Keithley 2425 100 W SourceMeter). Films were imaged with optical microscope (Olympus BX51) using brightfield setting, a reflected illuminator, objective lens (Olympus MPLAN 10×/0.25), and a digital camera (ARTRAY ARTCAM). The roughness of the insulator film was measured using atomic force microscopy (AFM) (Veeco Dimension 3100) operated in tapping mode (~260 kHz frequency, Nanosensors PPP-NCH-50 silicon probes).

3. Modeling

The PET substrate is stable at temperatures up to 150 °C; therefore the curing temperature should be kept below that. To estimate the influence of current density on the temperature rise at the conductor, Joule heating was modeled using a finite element method (Comsol Multiphysics®, version 3.5a from Comsol, Inc.) The simulation combined heat transfer model of the Heat Transfer Module and electrical conductivity model of the AC/DC Module.

Heat transfer in bulk material was modeled with the Fourier law of heat conduction [8]. The modeled domain is described in the inset of Fig. 2. The surface of the insulator was described with the heat-flux condition [9]. No inward heat flux was applied. The temperature of the bottom face of the PET substrate was forced to room temperature which corresponds to having a heat sink under the substrate during heating. The conductivity model was connected to the heat transfer model via heat source generated by the current.

The modeling results are illustrated in Fig. 2. They indicate that the substrate thickness has a strong effect on the temperature rise due to the relatively low thermal conductivity of PET. For a 125 μm thick substrate the temperature rise from 60 °C to 120 °C is achieved with current densities of $6.7–8.8 \times 10^9$ A/m^2. The thermal conductivity of PVP was considered to be constant in the model.

The model corresponds well to the observations; the insulator was heated in an oven and by Joule heating to temperatures near the boiling point of the PGMEA solvent (145–146 °C) in order to observe the formation of bubbles in the insulator due to boiling of the solvent. Comparison of temperatures in the oven and simulated temperatures corresponding to Joule heating currents showed that the error limit in the model is ca. 10 °C.

4. Results and discussion

Heating of PMMA causes solely evaporation of the solvent; no chemical reactions are taking place. In order to evaporate the solvent, heating current densities between 7.8 and 8.5×10^9 mA/m^2 were used. According to the modeling results these correspond to temperature between 100 °C and 130 °C. The curing time was long, 40 to 70 min, and the result was dependent on the rinsing step. The baked PMMA dissolves into the solvent, but significantly more slowly

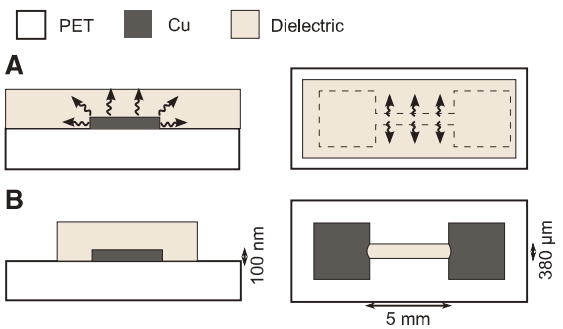

Fig. 1. Selective curing by Joule heating: a temperature rise at the conductor is caused by the electric current. (A) Insulator surrounding the conductor is cured and (B) residues can be rinsed away.

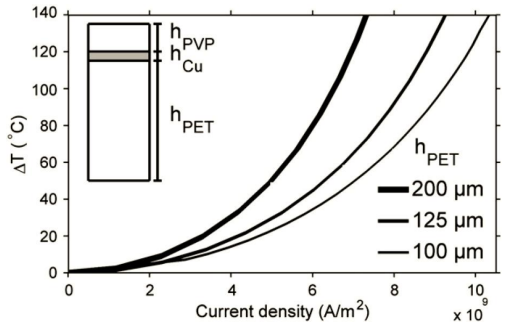

Fig. 2. Heat modeling was done for 100 nm thick copper conductor evaporated on PET substrate. Copper conductor is coated with 1 μm thick PVP-insulator. The curing temperature was estimated from modeling results. The substrate thickness has a strong effect on Joule Heating efficiency.

than non-baked PMMA. Due to this residual solubility, films made from the 5 wt.% PMMA formulation were too thin, and the insulator dissolved completely during the rinsing step. In the case of 15 wt.% PMMA a few ca. 2 μm thick insulating films were obtained, but the yield was low due to pinholes formed during the baking. The leakage current was 10^{-6} A/cm^2 at 20 V bias voltage.

The cross-linking of PVP and SC takes place through esterification of (4-vinylphenol) with acyl chlorides [10]. A cross-linking test for PVP was made by varying the Joule heating current. The dependence of capacitance on current with different parameters is illustrated in Fig. 3. Capacitances were measured at 40 MHz for which the measurement error was 2 pF. Thicknesses of the insulator layers are calculated from capacitance data using 4.2 as a material dielectric constant of cross-linked PVP [10].

Thicknesses of the single layer insulators deposited using a spin coating rate of 2000 rpm were between 150 nm and 200 nm. Insulators having thicknesses from 270 nm to 510 nm can be constructed with lower spin coating rate or by depositing multiple insulator layers. Microscope images of single and three layer insulators deposited with speed of 2000 rpm and cured with 8.2×10^9 A/m^2 current density are shown in Fig. 3A and B. The thickness of the multiple layer film is approximately the number of layers multiplied by the film thickness of one layer. With a speed of 500 rpm the film thickness is approximately 400 nm. Using a slower spin-coating rate enables the use of lower Joule heating current.

A slightly negative slope can be observed in the capacitance curve, which indicates increased film thickness as a function of current density. In the case of thicker insulator layers, a broadening of the temperature distribution causes widening of the cross-linked insulator over the wire edges. This can be prevented by minimizing the current and curing time.

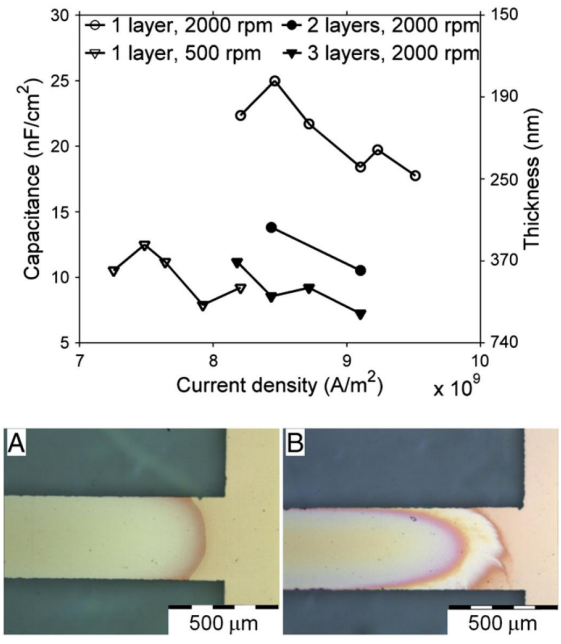

Fig. 3. Measured capacitances and calculated thicknesses as a function of heating current. Measurements were done for 1 to 3 layer PVP insulators cured for 5 min. Optical microscopy images of (A) a single insulator and (B) a three layer insulator coated with speed of 2000 rpm and cured with current density of 8.2×10^9 A/m^2.

Surface analysis with AFM revealed that insulator films cross-linked and patterned by Joule heating and washing with PGMEA are highly uniform and pinhole free layers with the RMS roughness values as low as 1.3–2.1 nm, slightly depending on the amount of insulator layers or applied current. In comparison, the RMS roughness of spin-coated PVP film was 0.9 nm after baking in the oven and 1.7 nm after PGMEA wash, which indicate that use of Joule heating and subsequent solvent wash very smooth dielectric surfaces can be obtained.

Leakage currents for the single layer insulator spin coating with 2000 rpm and the 3 layer insulator are presented in Fig. 4. Measured leakage currents for multiple layer insulators did not differ significantly from the data of single layer insulators spin coated with 500 rpm. Breakdown voltages were investigated applying DC bias voltages. We observed that 3 layer dielectrics could withstand voltages up to 60 V (field strength 140 MV/m) and single layer dielectrics up to 50 V (field strength 250 MV/m).

5. Conclusion

In this study, we have demonstrated a method for selective, self-aligned curing of polymeric insulators. A copper conductor is selectively heated by Joule heating creating a temperature rise at the conductor that cures the insulator and makes it insoluble. Curing is followed by a rinsing step that washes away uncured insulator. The method has been demonstrated for PMMA and cross-linkable PVP. Patterning of PMMA is dependent on control of the rinsing step, because curing of PMMA only slows down the dissolving of insulator. Heating of thermally cross-linkable dielectrics such as PVP/SC creates an insoluble insulator film. Optimization of curing parameters minimizes the widening of the insulator.

To conclude, we have demonstrated Joule heating as a way to perform self-aligned patterning of polymer dielectrics on metals. The patterned 3 layer film can withstand voltages up to 60 V without breakdown (field strength 140 MV/m) and if thermal cross-linking is used they are also highly resistant to solvent.

Acknowledgments

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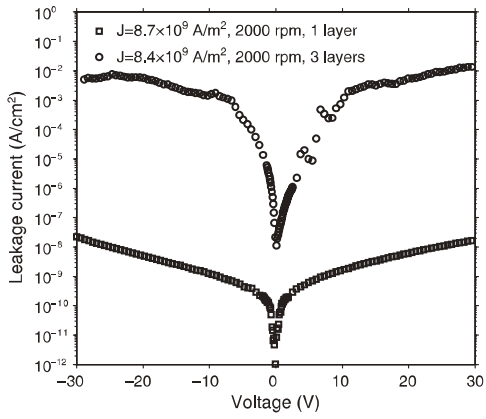

Fig. 4. Leakage current measurement for single and three layer PVP insulators with spin coating rate of 2000 rpm.

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Publication II

Janka M., Raumonen P., Tuukkanen S., Lupo D. Modelling of Joule heating based self-alignment method for metal grid line passivation, *MRS Proceedings*, 1628, 2014.

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Modelling of Joule heating based self-alignment method for metal grid line passivation

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ABSTRACT

A Joule heating based self-alignment method for solution-processable insulator structures has been modeled for the passivation of metal grid lines, for example for organic light emitting diodes or photovoltaic cells. To minimize overhang of the passivation layer from line edges, we have studied the Joule heating approach using solution-processable, cross-linkable polymer insulator films. Finite element simulations were performed to investigate the heating of the sample using glass and poly(ethylene terephthalate) (PET) substrates. The sample was at room temperature and the current was selected to induce a temperature of 410 K at the conductor. It was found that the selection of substrate material is crucial for the localization of cross-linking. For a PET substrate, the temperature gradient at the edge of the conductor is approximately twice the gradient for glass. As a result, using a glass substrate demands high selectivity from the polymer cross-linking, thus making PET a more suitable substrate material for our application. A flexible PET substrate is, in addition, compatible with roll-to-roll mass-manufacturing processes.

INTRODUCTION

The performance of organic photovoltaic devices (OPV) and light emitting diodes (OLED) is dependent on the device active area. Since known transparent conductors have a relatively high resistivity, the resistance of the transparent anode limits the power conversion efficiency in large devices for OPV applications and brightness homogeneity of OLEDs, due to the large lateral voltage drop inside the electrode. Integration of a metal grid with the transparent conductor improves the performance of OPVs and OLEDs. [1, 2]

Metal grids, however, decrease the device active area and thus they need to have low area coverage and high conductivity; they should be as narrow and thick as possible. This topology makes the anode and cathode prone to shorting. To avoid shorting, an insulating layer is put on top of the grid lines. This layer should cover only the grid lines in order to minimize the non-luminescent and non-illuminated areas; accurate alignment of the passivation layer is thus critical for maximizing the aperture ratio of the device. It is possible to use either photolithography or printing for the definition of the passivation layer. However, printing generally requires large overprinting and photolithography an additional alignment step, which is challenging when aiming at high throughput in roll-to-roll production. A self-alignment method offers better registration than printing without additional alignment steps.

Here we present finite element simulations of Joule heating in an aluminum grid line on PET and glass substrates. The aluminum line is heated by an electric current, causing a localized temperature increase in the vicinity of the conductor. The heat locally cures the insulator on top

of the the conductor, while it remains uncured and thus soluble farther away. The uncured dielectric can be rinsed away after crosslinking is completed. The method is described in detail in a previous publication [3]. Localization of the dielectric is dependent on the temperature distribution at the substrate and can be used as an estimate for the length overlap of the dielectric on a grid line. We investigate the effect of an indium tin oxide (ITO) layer on the diffusion of the heat.

The measured geometry of the device consists of domains with large dimensional differences (dimensions of the lines are 2 mm x 70 µm x 500 nm). Using this geometry for modelling would result in a very large mesh size, which would increase the modelling time, and in the worst case the mesh cannot be generated. To alleviate these mesh related problems, we model the problem using an equivalent problem with a "scaled geometry" that has greatly reduced dimensional differences [4].

THEORY

Modelling was carried using a finite element method (Comsol Multiphysics version 4.3 from Comsol, Inc.). The simulation combined a heat transfer model of the Heat Transfer Module and an electrical conductivity model of the AC/DC Module.

In order to investigate the effect of the transparent electrode on thermal diffusion, two geometries were compared; a plain substrate and a substrate coated with 150 nm thick ITO having a sheet resistance of 14 Ω/□. The substrate in the model is either 125 µm thick PET or 1 mm thick glass. A 500 nm thick and 70 µm wide aluminum line is placed either directly on substrate or on ITO. The length of the grid line is 2 mm on PET and 5 mm on glass. The uppermost is a 1 µm thick dielectric layer of poly(methyl methacrylate) (PMMA). Figure 1(a) illustrates the geometry used in the modelling.

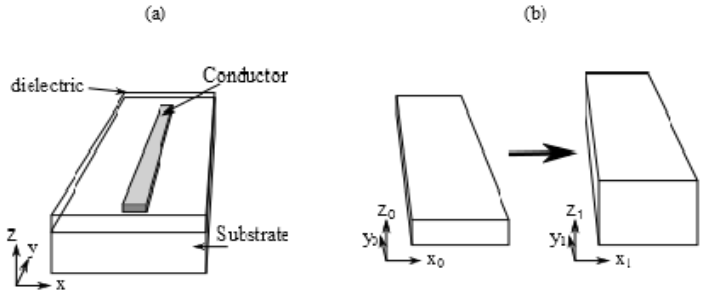

Figure 1. (a) Geometry of the model (dimensions not in scale) and (b) the scaling of the geometries

Since the dimensions of the different material blocks have large differences, the ratio between the dimensions is on the order of 10^3. The larger the dimensional differences are, the longer the calculation time is, and in the worst case a mesh cannot be generated. To overcome the problems caused by the dimensions, thicknesses of the materials are scaled so that there are no large differences between the dimensions. The scaled thicknesses are 50 µm for ITO, 100 µm for PMMA and 50 µm for Al. The scaling is illustrated in Figure 1 (b).

To transform the original problem to a new geometry so that the problems are equivalent, we need a mapping F between domains:

$$\mathbf{x}_1 = \mathrm{F}(\mathbf{x}_0) \tag{1}$$

The mapping F must be piecewise smooth and one-to-one, giving the correspondence between points and material blocks in the original geometry and the scaled geometry. Then, to make the problem with scaled geometry equivalent to the problem with original geometry, we need to modify the material parameters. This is done with the Jacobian matrix J of the mapping F. Material parameter matrices δ in the domains are related as follows [4]:

$$\delta_1 = \frac{1}{\det(J)} J \delta_0 J^T \tag{2}$$

where J^T and det(J) are the transpose and determinant of the Jacobian matrix. Each material was scaled separately in the model. Notice that material parameters in the scaled geometry are anisotropic.

Heat transfer in bulk material was modeled with the Fourier law of heat conduction [5], and the surface of the dielectric was described with a heat flux condition [6]. The bottom face of the substrate was set to room temperature corresponding to a situation where a heat sink is placed under the substrate, and the current was selected to induce a temperature of 410 K at the conductor. The modelling was done using stationary equations. This assumption is valid since the modelling indicated that the temperature stabilizes in less than a second and the heating time is a few minutes.

DISCUSSION

Even though the modeled grid line is only a few millimeters long the results are valid for longer lines as well. Heat conduction decreases the temperature at the ends of the conductor, thus temperature is not uniform along the conductor. The modeled conductor should be long enough that the ends do not have an effect on the temperature. For the glass substrate conductor length should be at least 5 mm and for PET 1 mm is enough. This result was used as a guideline for the geometry selection.

Scaling the thicknesses of the layer does not have a significant effect on the results. For example, increasing the scaled PMMA thickness 500 % decreased the calculated temperature at the conductor only 3 %. The mesh density, however, has an effect on the temperature gradient, which is the key parameter in investigating the selectivity of heating. In this sense the closer the scaled dimension are to each other, the better the gradient estimation is. Nevertheless, the scaling comes with a cost: The mesh is still generated as if there is no scaling in the geometry, which results in mesh elements that correspond to very elongated ones in the original geometry. This makes the condition number of the system matrix worse and can also affect the interpolation [7]. To improve this, the elements should be anisotropic, i.e. they should be elongated in the scaled geometry, in which case they correspond to “nice” elements in the original geometry. However, this option was not available in the version of the software used.

Figure 2 shows the temperature distribution along the x-axis for PET and glass substrates without and with ITO coating. Due to its higher thermal conductivity the glass substrate was

shown to be a more challenging material choice for Joule heating than PET. The temperature gradient near the conductor for plain glass is approximately 1 K/µm, while for plain PET substrates it is approximately 2 K/µm. This means lower localization of the cured dielectric. However, a glass substrate enables the use of higher temperatures, which decrease the time needed for the curing of the dielectric film. By a careful selection of the curing parameters it should be possible to create a well-aligned dielectric layer on glass.

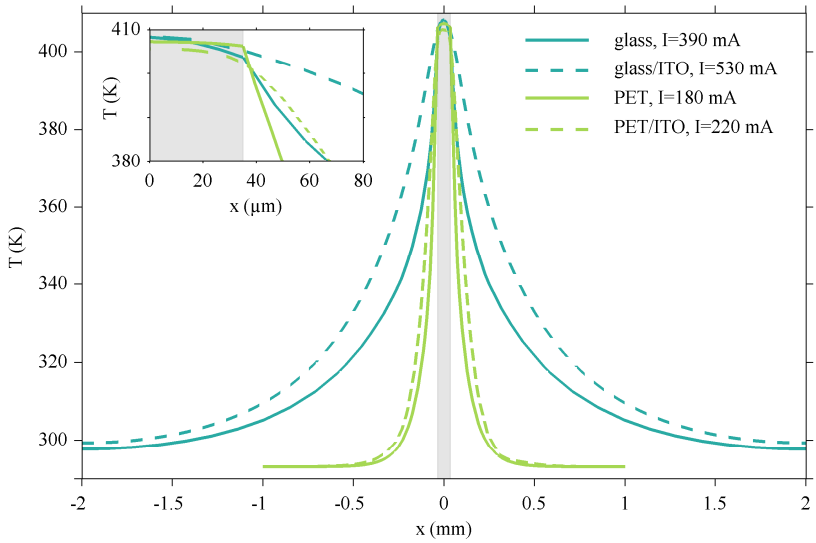

Figure 2. Temperature profile along x-axis (perpendicular to the conductor). The conductor is indicated with the gray bar at graph. Inset: magnification near the edge of the conductor.

The inset of figure 2 shows the magnification of the temperature profile near the conductor edge. Whereas the temperature gradient with the plain substrates is highest at the edge of the conductor, ITO shifts the maximum gradient further away from the edge. At the edge of the conductor temperature gradient for the PET/ITO substrate is 0.6 K/µm and for glass/ITO 0.2 K/µm. This indicates a need for careful optimization of the curing parameters in order to achieve high locality of the dielectric.

An ITO layer on PET does not have a significant effect on the distance from the conductor where the heat is stabilized to room temperature. For the glass substrates, the temperature is stabilized at the distance of 2 mm from the conductor, whereas for PET substrate the corresponding distance is only 0.5 mm. Based on this it can be estimated that for multiple conductors heated simultaneously, the heating selectivity does not degrade when the conductors are separated at least by the distance needed for the temperature to reach room temperature. For PET this distance is 1 mm and for glass it is 4 mm. This, however, should be verified by modelling multiple gridlines.

Higher current is needed to create sufficient temperature on a glass substrate than on a PET substrate. This is because a large area of glass is heated during Joule heating. To reach a temperature of approximately 410 K, the Joule heating current for glass substrate is 390 mA

whereas the corresponding current for PET is 180 mA. The ITO layer increases the required current. For PET substrate, the ITO layer increases the required current to 220 mA, (approximately 20 % increase) and for glass/ITO substrate 530mA (35 % increase). The increase results from current flowing in the ITO, as well as the increased heat spreading into the substrate. The actual current that passes through the conductor is 204 mA for the ITO/PET substrate and 452 mA for the ITO/glass substrate as the rest of the current flows through ITO. Even though a small current flows in the ITO, resistive heating in ITO is negligible.

The degree of heat localization is affected by the thermal conductivity of the materials under the conductor. The differences between the substrate materials are explained by the 10 times higher thermal conductivity of compared to PET. [8, 9] Thermal conductivity of ITO is, however, 100 times higher than thermal conductivity of PET.[10] Based on these values it is surprising how small an effect the ITO layer on PET has on the heat spreading. This predicts that heat tends to move to air rather than spread along the thin layer of ITO. By decreasing the ITO thickness it might be possible to increase the temperature gradient at the edge of the conductor. However, decreasing the ITO thickness decreases its sheet resistance and thus affects negatively the device performance. Other transparent conductors might offer better heat localization during Joule heating. For example thermal conductivity of PEDOT:PSS (poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate)) is 0.17 $Wm^{-1}K^{-1}$ [11]. As a comparison, the corresponding value for PET is 0.15 [9], predicting that with a PEDOT:PSS transparent anode layer, the localization of the passivation should not differ from that of plain PET. The effect of the ITO thickness as well as PEDOT:PSS should be studied further.

CONCLUSIONS

Self-aligned passivation of anode grid lines for OPV and OLED applications using Joule heating was studied by a finite-element method. Suitability of glass and PET substrate for the Joule heating method was compared. Due to large dimensional differences in the material layers, the mesh can be too large or impossible to generate. Therefore the geometry of the model used for computations was scaled to reduce the dimensional differences.

Joule heating on glass consumes more energy than on PET, since higher current is required to create sufficient temperature due to the higher thermal conductivity. More heat is conducted into a glass substrate than into PET, where less energy is consumed to heat the substrate. When heating multiple conductors simultaneously, the heating area increases, and more heat will be transferred in to the substrate. With the substrate having higher tendency to store heat this may have a negative effect on the localization. We conclude that PET is a more suitable material for Joule heating method than glass. An ITO layer on PET decreases the temperature gradient at vicinity of the conductor edge, demanding more careful optimization of curing parameters.

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Publication III

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Optimization of large-area OLED current distribution grids with self-aligned passivation

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ABSTRACT

The luminance homogeneity of large-area organic light emitting diodes (OLEDs) is limited by the sheet resistance of the transparent electrode. A large lateral voltage drop inside the electrode and thus brightness inhomogeneity result from the high sheet resistance of transparent conductors. To improve sheet resistance, a low-resistance metal grid is often included. To prevent shorting, the grid needs to be passivated. However, since passivation further decreases the device active area, accurate alignment of the passivation layer is crucial. We report simulations of a Joule-heating-based self-alignment method for the passivation layer. The Joule heating model was divided into two sub-models: a current model to study current distribution on grid scale during Joule heating, and thermoelectric model to study heat transfer in the system. Grid design rules – minimum line pitch and the geometry of the grid – necessary for a successful Joule heating process were studied. The line group design was found to be the best option for a current distribution grid. The minimum line pitch limited by heat transfer was 0.8 mm on an indium tin oxide (ITO) coated polyethylene terephthalate (PET) substrate. With the line group design, maximum luminance output was achieved with a pitch of 4 mm, when the sheet resistance of the metal lines was 0.01 Ω/□. This fulfils the demands placed by the Joule heating process.

1. Introduction

As the performance of organic light emitting devices (OLEDs) has improved [1], OLEDs have become potential candidates for flat, flexible large-area lighting sources [2]. In addition to increased device performance, life cycle energy efficiency can be improved with low energy intensity manufacturing [3]. Manufacturing costs can be further cut by reducing process complexity, for example by using high volume low-resolution, self-aligning processes to replace low-volume high-resolution registration.

An issue for large-area OLEDs is the limited conductivity of the transparent anode, which causes a lateral voltage drop across the surface of the OLED and thus leads to inhomogeneous light emission [4]. Commonly, conductivity is increased by integrating a metal grid with the transparent electrode. Because the grid lines reduce the active area of the device, it is desirable to use narrow, thick metal lines for high conductivity and minimal drop in the device luminance area [5]. Thick metal lines, however, must be passivated by an insulator to prevent shorting of the lines and the cathode due to the extremely thin active layer of the OLED between them. Because this passivating layer further lowers the device luminescent area, the layer must be accurately aligned to maximize the aperture ratio (fraction of the active device area) of the device. The passivating layer

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can be a printed or photo-lithographically aligned polymer dielectric. Printing, however, generally requires significant overprinting, especially if flexible substrates are used, and this can lead to unacceptably low aperture ratios. Photolithography, in addition to being relatively expensive, requires an additional alignment step, which is challenging when high throughput production is intended, and it cannot easily be corrected for substrate distortion during processing. We have previously shown that conductive lines can be passivated with excellent registration using a self-alignment approach based on Joule heating [6]. In this paper, we examine the possibility of using the same approach to passivating current distribution grid lines for OLEDs.

The self-alignment process is fairly simple. An electric current is passed through a metal line, and the generated heat cross-links the polymer insulator near the line. The uncured polymer farther away remains soluble and can be rinsed away after curing [6]. The spatial resolution of passivation depends on the selectivity of the curing temperature for the cross-linked polymer, the thermal properties of the substrate and transparent anode material, and the grid line design.

This study introduces finite element simulation of a Joule-heating-based self-alignment method. The Joule heating process was modelled with two sub-models: a current model and a thermoelectric model. The grid type was selected using the current model, based on the assumption that the current should be equal in all lines heated for an equal amount of time. The thermoelectric model was applied to a small subsection of the grid to study heat localization in a line and line groups. When the line pitch in a grid is small, the adjacent lines heat each other during Joule heating, resulting in decreased heat localization. Thus the minimum line pitch, which has no effect on heat localization, was estimated using the thermoelectric model. The reliability of this model was validated by comparing modelling and experimental data on Joule heating.

The Joule heating method limits the choice of grid designs. The luminance distribution of the OLED was simulated for a grid design suitable for Joule heating and compared with a square grid structure. The OLED was modelled using literature data for j–V characteristics.

2. Modelling

The passivation process of the metal grid lines of a bottom emitting OLED was studied. The Joule heating process limits the choice of the design of the current distribution grid. For minimization of the overhang of the passivation layer, the temperature and thus the current should be equal in each line heated for an equal amount of time. To select a grid system, we studied the process on grid scale with the current model. Though the model gives a rough selection of grid types, it provides no information on the curing locality. Heat transfer limits the minimum distance between the grid lines in that when the line pitch is small, adjacent lines heat each other. By choosing various substrate and anode materials, the heat locality can be controlled. Consequently, we applied thermoelectric modelling to a small subsection of the grid to study the locality of heating.

To estimate how grid design affects OLED luminance, we simulated voltage distribution in a square grid and a line group. All simulations were carried out using a finite element method implemented with commercial software (Comsol Multiphysics version 4.3 from Comsol Inc.) (overview of modelling shown in Fig. 1).

2.1. Joule heating

The modelled geometry of the grid system consisted of domains of large dimensional differences; in width and height the grid lines were from three to four orders of magnitude smaller than in length. In addition, the grid system consisted of dozens of lines. Modelling Joule heating with this geometry would have resulted in a very large mesh and would have added to modelling time, or in the worst case a mesh could not have been generated at all. The problem was thus divided into separate subsystems: a 2D current grid system model and a 3D thermoelectric grid subsections model. To further cut down on modelling time and to improve the properties of the mesh, we modelled the thermoelectric problem using an equivalent problem with a scaled geometry with greatly reduced dimensional differences [7,8].

2.1.1. Current model

Current was modelled to compare different grid types: hexagon grid, square grid, and line group (Fig. 2). Hexagon and square grid geometries create good voltage homogeneity at a transparent anode [9,5], and the line group design is the most suitable for Joule heating. The current model gives no information about the curing locality, but it describes how the current flows in a grid system. For successful Joule heating, the current should be equal in each line heated for an equal amount of time.

The current was calculated using Ohms law with an electrical conductivity model of the AC/DC Module. The grid lines where 70 μm wide and 500 nm thick aluminium lines. For a transparent anode, 150 nm thick ITO with a sheet resistance of 14 Ω/□ was used. The thickness was used to calculate the sheet resistance of the materials for the 2D model.

2.1.2. Thermoelectric model

Because the Joule heating model combined thermal and electrical models, it required large calculation capacity, and could not be used for large areas, only a small subsection of the grids was modelled thermoelectrically. In the model, heat transfer in the bulk material was described with the Fourier law of heat conduction [10] and the surface of the dielectric with a heat flux condition [11]. The bottom face of the substrate was forced to room temperature, corresponding to a heat sink being placed under the substrate. Stationary equations were applied in the model, because the temperature stabilized in less than a second, whereas the heating time was a few minutes.

Simulations combined a heat transfer model of the Heat Transfer module and an electrical conductivity model of

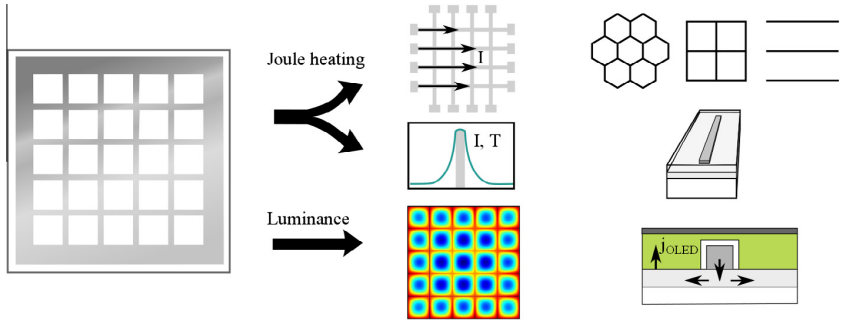

Fig. 1. A Joule-heating-based passivation process was studied by modelling to verify the design criteria for a current distribution grid. The Joule heating model was divided into two subsystems: a 2D current model of the grid to compare different grid types and a 3D thermoelectric model of subsections of the grid to study heat transfer during Joule heating. Finally, the effect of the selected current distribution grid design on luminance homogeneity was simulated.

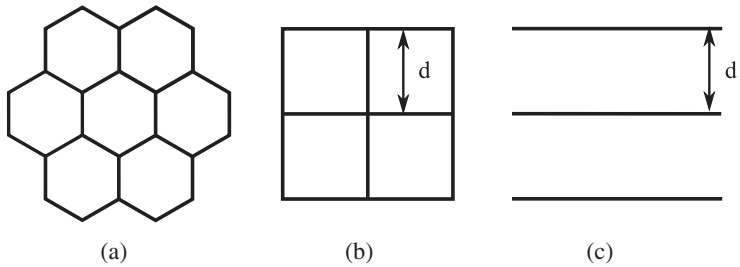

Fig. 2. Designs used to model current: (a) hexagon grid, (b) square grid, and (c) line group.

the AC/DC Module. The latter was connected to the former with a heat source generated by electrical power.

To reduce the dimensional differences of the materials, the anode layer and the metal lines were scaled to a thickness of 50 μm and the dielectric layer to 100 μm, whereas the 125 μm polyethylene terephthalate (PET) substrate was not scaled for thickness. Fig. 3 shows the schematics of the geometry used in the Joule heating model. The rectangular cross-section of the metal line in the figure represents evaporated lines, and this geometry was used in the model unless otherwise indicated. Due to the surface tension of the ink, the cross-section of the printed lines is best described as a half-ellipse.

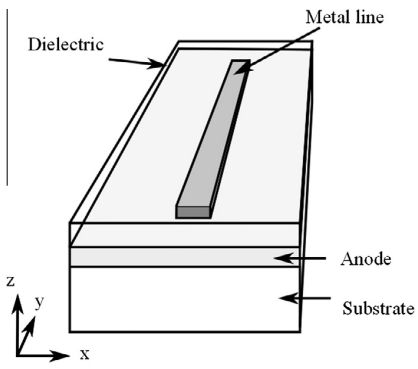

Fig. 3. Geometry of the Joule heating model. Dimensions are not to scale.

The scaled geometry corresponds to a real system where the transparent anode layer is either 150 nm thick indium tin oxide (ITO) or 100 nm thick poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS). Unless otherwise indicated, 70 μm wide, 500 nm thick aluminium lines are used as a current distribution grid, and the uppermost layer was a 1 μm thick dielectric layer of poly(methyl methacrylate) (PMMA).

Anode sheet resistances were chosen to be 14 Ω/□ for ITO and 200 Ω/□ for PEDOT:PSS. The thermal conductivities of PET, ITO, and PEDOT:PSS were 0.15 $W\,m^{-1}\,K^{-1}$ [12], 10.2 $W\,m^{-1}\,K^{-1}$ [13], and 0.17 $W\,m^{-1}\,K^{-1}$ [14], respectively. Aluminium and PMMA properties were taken as provided by the Comsol Multiphysics material library. As long as the electrical and thermal conductivities of the grid lines are significantly higher than those of the transparent electrode, they have no effect on the localization of heating, and thus the choice of material is not critical.

To validate thermoelectrical simulations, a temperature validation test was run on the PET substrate and the 360 μm wide, 100 nm thick evaporated copper lines. A measured sheet resistance of 0.3 Ω/□ was used in the model.

2.2. Voltage distribution in a bottom emitting OLED

The electrical model for an OLED calculated the voltage loss in the OLED during operation. The following approximations were used in the model:

- The cathode was grounded, and there is no voltage drop in it: $V_c = 0$.
- The anode and the metal grid potential were independent of the z-direction: $V_a(x,y,z) = V_a(x,y)$.
- In locations where the grid and anode overlapped, the grid potential equalled the transparent electrode potential: $V_g = V_a$.

Voltage inside the anode was modelled using a 2D-model for an OLED. According to Neyts et al. [9], the current density pointing out to the anode plane in a stationary situation is

$$\frac{1}{R(x,y)}\nabla^2 V_a = -j_z(x,y,V_a), \tag{1}$$

where $R(x,y)$ and V_a are the sheet resistance and the voltage of the anode. The anode sheet resistance can be approximated to the grid sheet resistance R_g in locations of grid lines and to the sheet resistance of the transparent conductor R_a where there is no grid. The source term j_z in the continuity equation is the current density in the z-direction flowing away from the anode.

When no grid is present, the current flows trough the light emitting layers $j_z = j_{OLED}$, as shown in Fig. 4. The grid lines are passivated with a dielectric layer, and thus the current flows to the transparent anode layer below the metal line instead of the light emitting layers. The overhang of the dielectric layer was approximated to zero for simplicity. In the 2-dimensional model, j_z in the grid location is related to the current flowing in the transparent conductor as follows: $j_z = h_a/w_g j_a$, where j_a is the anode current in the x, y-direction. Since j_a is proportional to the anode voltage gradient, and since $V_g = V_a$ at the grid, the continuity equation becomes

$$\frac{R_a}{R_g}\nabla^2 V_a = -\frac{1}{w_g}\|V_a\|. \tag{2}$$

Voltage distribution simulations were performed using Poissons equations of the Mathematics module. At the edges of the domain, the Dirichlet boundary condition was applied to describe the operational voltage on the busbars of the OLED. We assumed no voltage loss in the busbars.

The voltage distribution model exploited the same parameters as the Joule heating model, except for the sheet resistance of the metal lines, which was 0.01 Ω/□ corresponding to approximately 3 μm thick evaporate aluminium or copper lines. The width of the lines was 70 μm as

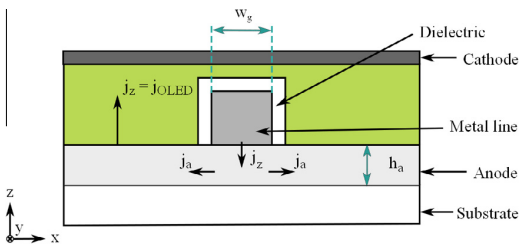

Fig. 4. Cross-section of an OLED in the luminance model.

in the Joule heating model. As noted above, the thickness and conductivity of the metal are not critical for the selectivity of the Joule heating process. The OLED current was modelled as a linear function of an anode voltage $j_{OLED} = (V_a - V_{th})/r$, where the threshold voltage $V_{th} = 4.4$ V and $r = 0.012$ m²/AV [15]. Luminance was approximated to be a linear function of the anode voltage with a slope of 2000 Cd m^{-2} V^{-1} and an edge luminance of 1200 Cd [9].

3. Results and discussion

The Joule heating of the current distribution grid was studied first by using a current model for selecting a grid system. Heating a small subsection of the grid was described with a thermoelectric model, which was used to study heat localization and to estimate the required line pitch. Finally, the design criteria, grid type, and line pitch derived from the Joule heating models were qualified by simulating emission homogeneity with an OLED model using the current distribution grid.

3.1. Current model

Current was modelled in different grid systems to determine the path it tends to flow. The following grid types were compared: hexagon grid, square grid, and line group (see Fig. 1). Significant in all these cases is that the shunt lines circulating the active area of the OLED must be deposited after Joule heating. Otherwise the current during Joule heating flows through the shunt lines, bypassing the grid itself. The current should be equal in all lines for each line to have homogeneous temperature during Joule heating.

3.1.1. Hexagon grid

To avoid a current in the shunt lines, each conductor in hexagonal grid systems needs separate pads, and the vertical and horizontal grid lines must be heated separately. In a hexagonal grid design, the magnitude of the current in each grid line depends on the location of the line and the direction of heating. The current varies greatly, about 25%. With this design, Joule heating results in large variation in the overhang of the dielectric.

3.1.2. Square grid

Like the hexagon grid, the square grid requires separate pads for each line to prevent the Joule heating current bypassing the grid. Near the pads, the current is about 15% higher than elsewhere, where it varies only 3%. However, heat conduction decreases the temperature near the pad areas and thus partially compensates for the effect of increased current. The square grid offers better current homogeneity than the hexagon grid. Because the current depends on the design of the grid line and the grid itself, the results are only suggestive. However, they point toward the suitability and shortcomings of the square grid design.

3.1.3. Line group

The line group is the most promising design for Joule heating. Since all lines are electrically connected only by shunt lines, only one heating step is needed. Shunt lines parallel to grid lines must be printed after Joule heating, but perpendicular lines can be printed in one pass, which makes it easier here to contact the grid lines during Joule heating than in the square and hexagon grid structures. Furthermore, the current is equal in all lines during Joule heating.

3.2. Thermoelectric model and dielectric curing

Thermoelectric modelling was applied only to single metal lines and a small subsection of the line group design and verified with the current model to be suitable for Joule heating.

3.2.1. Single line with different anode materials

In the single line case, two geometries were compared, a plain substrate and a substrate coated with a transparent conductive layer to study the effect of the transparent electrode on thermal diffusion. Because the width or the electrical and thermal conductivities of the line had no effect on the selectivity of heating, a 500 nm thick aluminium line was chosen as an example grid line. The line was placed either directly on the substrate or on the transparent electrode.

Fig. 5 shows the temperature distribution along the *x*-axis with and without ITO or PEDOT:PSS coating. The inset in the figure shows the magnification of the temperature profile near the conductor edge. The temperature gradient, which is an indicator of heat locality, was highest at the edge of the conductor with the plain substrate and the PEDOT:PSS coated substrate, whereas ITO shifted the maximum gradient further away from the edge. At the edge of the conductor, the temperature gradient for both PET and PET/PEDOT:PSS substrates was approximately 2 K/μm and for the PET/ITO substrate 0.6 K/μm.

With a current of 180 mA, the temperature at the conductor on the PET substrate was 407 K. When PET was coated with a PEDOT:PSS layer, the temperature dropped

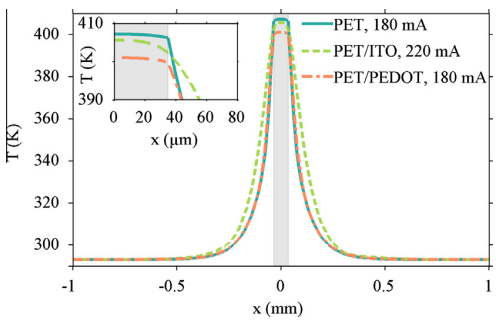

Fig. 5. Temperature profile along the *x*-axis (perpendicular to the conductor) for PET, PET/ITO, and PET/PEDOT:PSS substrates. The conductor is indicated with a grey bar. Inset: magnification near the edge of the conductor.

to 401 K. This is a result from a small, 1 mA current flowing though the transparent conductor layer instead of the conductor. The ITO layer increased the required current to 220 mA, resulting from increased heat spreading into the substrate and from 16 mA of current flowing in the ITO. Though a small current flowed in the ITO, its resistive heating remained negligible due to a very low current density.

The thermal conductivities of the materials under the conductor affect the degree of heat localization. ITO, however, had a 100 times higher thermal conductivity than PET [12,13]. Because the cross-sectional area of ITO was smaller than the surface area of the conductor, the horizontal heat flux along ITO was smaller than that in the much thicker substrate and dielectric. In comparison, the thermal conductivities of PEDOT:PSS and PET were similar [12,14], and thus the PEDOT:PSS layer had no effect on heat localization.

Variation in the current affects the length of the dielectric overhang through a change in the peak temperature and thus the width at which the curing temperature is reached. For example, a 1% increase in current increased the overhang by about 5 μm, a 10% increase in the shadow area on the PET/ITO substrate. The corresponding increase for the PET/PEDOT:PSS substrate was 1.5 μm. The current model estimated a 3% variation in current in the square grid resulting from its design, which would translate into about 15 μm variance in the dielectric overhang. In conclusion, the line group offers much better homogeneity of dielectric overhang and a considerably lower shadow area with the same grid coverage.

3.2.2. Line group

Simultaneous Joule heating of line groups was modelled for PET and ITO/PET substrates. The temperature should be equal in all lines during Joule heating. If the heating of a line affects the temperature of adjacent lines, the temperature at the border of the anode is lower than in the centre. This results in an uneven overhang of the dielectric, or, in the worst case, the lines at the border not being fully passivated. A small distance between the lines also significantly increases the temperature at the PET substrate between the conductors, resulting in less localized heating.

The number of lines was increased until the maximum temperature in the line group saturated to show trends in temperature distribution. The inset in Fig. 6 shows the temperature profile in a group of three lines on a PET substrate. When the distance between the lines was 0.3 mm, the central conductor heated the most. With this line pitch, the model for an individual line does not describe line groups accurately. For line distances from 0.4 mm to 1 mm, the temperature at the conductor depended slightly on the pitch, but in all lines it was equal. However, the maximum temperature in the line group saturated at three conductors when the line pitch was 0.4 mm or more, as seen in Fig. 6. The one-line model thus describes accurately the Joule heating of a line group. Though the substrate in the model was plain PET, the results apply to PET/PEDOT:PSS substrates as well, as can be seen in Fig. 5.

For comparison, simulations were repeated for PET covered with ITO. ITO increases heat dissipation into the substrate and thus the minimum distance between conductors

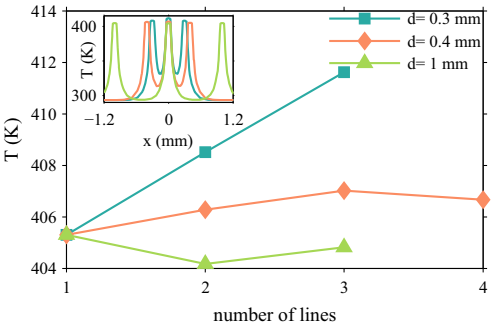

Fig. 6. Maximum temperature in a line group on the PET substrate as a function of the number of lines with a different line pitch d. Inset: temperature profile of a group of three lines.

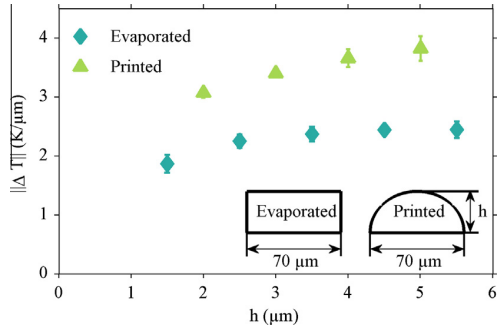

Fig. 8. Comparison of the localization of heating in evaporated and printed lines. Because the results varied only slightly, error bars are not visible at all data points.

that can be used for homogeneous heating. At 0.8 mm, the temperature increased slightly when the number of the conductor increased. However, the temperature saturated at four conductors and was equal in all conductors. For an ITO/PET substrate, the distance between the lines should be more than 0.8 mm. The results are shown in Fig. 7.

3.2.3. Printed lines

For large-area manufacturing, the optimum approach is to print the current distribution grid. Consequently, evaporated and printed lines were compared. The former were modelled with a rectangular cross-section, and the cross section of the latter was approximated to a half ellipse, as shown in the inset of Fig. 8.

The thickness of the evaporated lines was swept from 1.5 µm to 5.5 µm and for printed lines from 1 µm to 5 µm. The dielectric thickness was a constant 6 µm in all simulations. Because the temperature gradient at the edge of the conductor is a good proxy for heating selectivity, the temperature gradients of the printed and evaporated line were compared as a function of thickness (Fig. 8). The gradient was calculated at five locations for variance in it. Because the temperature at the line was within 6 K, its effect on the gradient was negligible. The figure helps conclude that the thickness of the line increases the temperature gradient only slightly, whereas the shape of the conductor has a clear effect on the gradient. Thus the size of the overhanging area is not as prone to changes in the cross-sectional area of printed lines as it is to changes in evaporated lines.

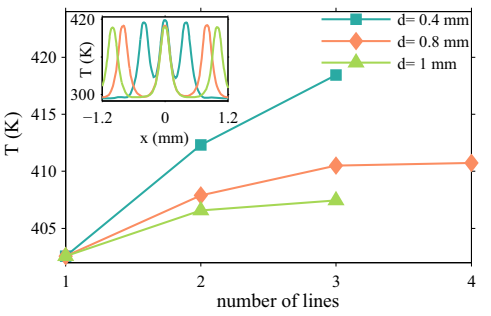

Fig. 7. Maximum temperature in a line group on the PET/ITO substrate as a function of the number of lines with a different line pitch d. Inset: temperature profile of a group of three lines.

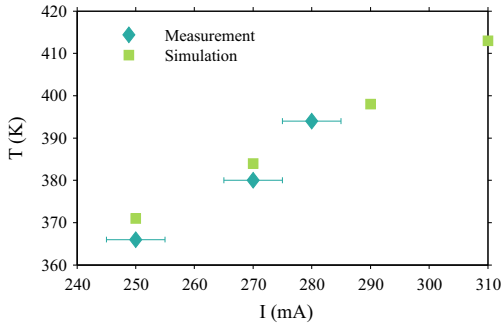

Fig. 9. Comparison of measurements and simulation for Joule heating maximum temperature.

3.3. Validation of the Joule heating model

To validate the Joule heating model, we measured the temperature with indication liquids (Tempilaq G from Tempil). Indication liquid was applied to the evaporated copper lines on PET substrates. After the film had dried, electric current was used to heat the copper line. The current was increased until the film melted and indicated the temperature reached. Measurement was made with three different indication liquids with melting points of 366 K, 380 K, and 394 K.

Measurements and simulation are compared in Fig. 9. The measurement results are only approximate, since the grain size of the indicating material was of the same magnitude as the width of the conductor. The accuracy of the current adjustment was approximately 10 mA. However, according the results, simulation corresponded well with the experimental data.

3.4. Emission homogeneity of grid designs

To compare the line group with a more common square grid geometry in OLED operation, a 10 × 10 cm^2 size panel was analyzed for luminance loss. An operational voltage of 5 V was applied to the edges of the panel, and the relative average luminance L_{avg}/L_{edge} was calculated. L_{edge} was the luminance at the edge of the panels, and L_{avg} was the average luminance of the panel. The sheet resistance of the lines in the model was 0.01 Ω/□ with the corresponding evaporated metal lines having a thickness of approximately of 3 μm. The width of the lines was 70 μm.

Fig. 10 shows the simulation data on relative average luminance versus percentage grid area coverage. The line group and square grid on ITO are compared. When the line pitch is small, in other words, when the area coverage is high, loss in luminance is dominated by line shadows instead of the voltage loss in the panel. The dashed line in the plot represents the light transmissivity of the grid. The maximum average luminance for the line group and square grid on ITO was approximately 98% of the edge luminance in an area coverage of approximately 1.3% for the square grid and 1.7% for the line group. The coverage values correspond to a line pitch of 4 mm for the line groups and 1 cm for the square grid. Grid shape had no effect on the average luminance of the panel. A less conductive transparent anode PEDOT:PSS decreased the average luminance, when the area coverage was smaller than 2% (line pitch more than 4 mm). Optimum line spacing values were from 2 to 4 mm.

The model assumed a negligible overhang for the dielectric, which does not exactly correspond to a real situation. The area of the overhang lowers the average luminance, and the optimum area coverage is smaller than that estimated by the model, because the shadows of the lines are larger than without a dielectric overhang.

Fig. 11 shows the relative luminance of square grid and line group OLED panels. The line group and the square grid had a metal line area coverage of 0.63% and 0.56% (line pitch of 1 cm for line group and 2 cm for square grid) and an average luminance of 98% and 97%, respectively. The luminance of the square grid had a rotational symmetry of 90°, which was not the case with the line group. Symmetry allows more freedom in placing the panels in consumer applications.

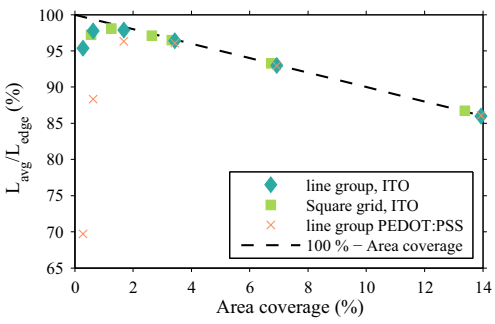

Fig. 10. Relative average luminance for the line group on ITO and PEDOT:PSS and the square grid on ITO as a function of area coverage %.

In conclusion, compared to the square grid structure, the line group design does not lower OLED performance, and thus Joule heating is well suited for passivating current distribution grids. However, if the increase in the variation of the Joule heating current and further in the dielectric overhang resulting from the shape of the square grid is taken into account, the average luminance of an OLED panel will drop from that of a line group OLED panel. We can thus conclude that a line group OLED panel offers better luminance output than a square grid panel, when the dielectric is patterned with Joule heating. In addition to better luminance output the line group is simple to manufacture.

The optimum line pitch on ITO, in terms of luminance, is 4 mm. According to the Joule heating simulations, the line pitch should be more than 0.8 mm to achieve homogeneous temperature in all lines during heating. Although the optimum line pitch is dependent on the OLED properties and thus the value calculated using an example OLED does not describe all OLEDs, the result further indicates the compatibility of Joule heating with current distribution grids.

The Joule heating process requires four process steps: applying the dielectric, curing and development, and also grid structure needs to be patterned in two pieces, since the shunt lines parallel to metal lines need to be deposited after the Joule heating step. None of these steps require vacuum processes or time consuming and expensive microscale registration while achieving very low unnecessary loss of luminance due to for example overhangs. Thus the Joule heating process has the potential for cost effective industrial scale production.

By comparison, a printed passivation layer is simpler to produce; the metal grid and shunt lines can be printed simultaneously and the applying the passivation layer requires only one step. However, due to limits of registration, printing of the passivation layer generally requires significant overprinting. Thus the advantage of the printing in cost effectiveness is lost in the decrease of the OLED active area and thus the performance.

Photolithography requires the same number of process steps as Joule heating, but the alignment step is challenging in high throughput production. Furthermore, photolithography is not a convenient method to passivate printed grid lines. Large overhang of the passivation layer is required, since the width of the printed lines is not uniform and accurate.

Though the Joule heating places requirement for the grid design, the best design, a line group, in terms of Joule heating, is also the simplest to manufacture. It also creates uniform light output, and does not decrease the cost-effectiveness of the OLED.

4. Summary

A self-alignment passivation method for an OLED current distribution grid was studied by modelling. A model that combines both electrical conductivity and heat

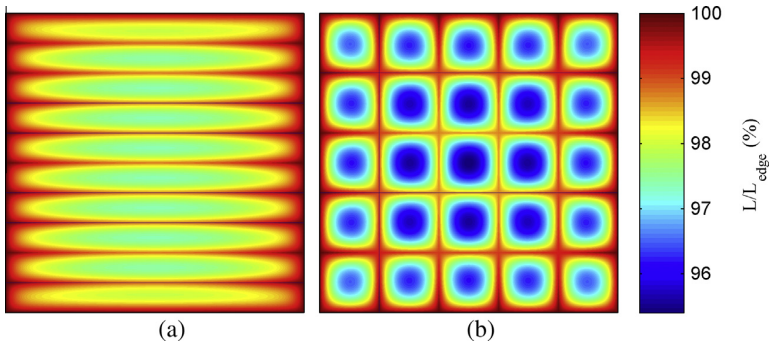

Fig. 11. Relative luminance of OLED structures with (a) a line group and (b) a square grid. Note the narrow scale on the colorbar to bring out the variation in luminance. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

transfer models requires large calculation capacity and cannot be used for large areas. Thus the Joule heating problem was divided into a current model on grid scale and a thermoelectric model of a subsection of the grid. Use of combined current and electrical modelling gave a good understanding of Joule heating on grid scale.

The current model narrowed the selection of three grid designs to one, the line group design. With this design, the Joule heating current was divided evenly with all the lines exhibiting uniform temperature. Thus the variance in the overhang of the passivation layer depended only on the variation in line width. The distance between the lines in a group should be more than 0.8 mm to guarantee that heating all the lines simultaneously does not affect the locality of the heat nor the temperature at the grid lines.

To compare the luminance of an OLED with a line group as a current distribution grid to a common square grid structure, the OLED anode was analyzed for voltage drop. The line group design was found not to lower OLED performance significantly compared to a square grid structure. Consequently, while it limits the choice of grid design, Joule heating is well suited for passivating current distribution grids. The optimum line spacing for line groups on an ITO anode is approximately 4 mm depending on the OLED parameters, which is more than the required minimum distance estimated by the Joule heating model. It has been demonstrated in an earlier study that the dielectric films of thickness of approximately 200 nm patterned using Joule heating process withstands voltages up to 30 V without breakdown [6]. The requirements of OLED for the voltage resistance are significantly smaller than that. In conclusion, Joule heating is a suitable method for passivating current distribution grid lines.

Acknowledgements

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Publication IV

Janka M., Gierth R., Rubingh J.-E., Abendroth M., Eggert M., Moet D.J.D., Lupo D. Passivation of OLED anode grid lines by pulsed Joule heating, *Applied Physics Letters* 107(10): 103304, 2015.

Passivation of organic light emitting diode anode grid lines by pulsed Joule heating

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We report the self-aligned passivation of a current distribution grid for an organic light emitting diode (OLED) anode using a pulsed Joule heating method to align the passivation layer accurately on the metal grid. This method involves passing an electric current through the grid to cure a polymer dielectric. Uncured polymer is then rinsed away, leaving a patterned dielectric layer that conforms to the shape of the grid lines. To enhance the accuracy of the alignment, heat conduction into the substrate and the transparent electrode is limited by using short current pulses instead of a constant current. Excellent alignment accuracy of the dielectric layer on printed metal grid lines has been achieved, with a typical 4-μm dielectric overhang. In addition to good accuracy, pulsed Joule heating significantly cuts down process time and energy consumption compared to heating with a constant current. The feasibility of using a printed current distribution grid and Joule heating was demonstrated in an OLED device.
[http://dx.doi.org/10.1063/1.4930883]

In recent years, organic light emitting diode (OLED) technology has developed rapidly, enabling thin, flexible, and lightweight large-area light sources or displays. The resistivity of the transparent electrode limits the size of the OLED panel, because lighting applications require homogeneous luminance over a large area.[1] A thick and narrow metal grid is typically integrated with the transparent electrode to decrease the electrode's resistivity.[2] To prevent a short circuit between the cathode and the anode of the device, thick metal lines must be passivated with an insulator. Since the grid lines and the passivation layer decrease the active area of the device, it is essential to align the passivation layer accurately onto the grid lines to minimize loss in active area.

Printing and photolithography have been used to pattern the passivation layer. Printing methods are cost-effective and involve the fewest process stages of all passivation methods. They have the drawback, however, of relatively poor layer-to-layer registration accuracies,[3–5] which necessitates a significant overhang over the edges of the grid line to ensure full coverage. Therefore, a large active area is lost if the passivation layer is printed. In contrast, the layer-to-layer registration accuracy reported for roll-to-roll photolithography is 1 μm.[6] However, photolithography is a relatively expensive process and requires an additional alignment step, which is challenging if high throughput production is intended. Furthermore, if the target line is not well defined, which is the case with printed lines, a large overhang is required to fully cover the grid line.

To create an accurately aligned passivation layer by low cost methods, we have studied self-alignment passivation based on Joule heating. In this method, an electric current is passed through the grid lines to heat them selectively. The heat generated cross-links a polymer insulator near the lines and uncured polymer is rinsed away after curing. As a result, insulator patterns are aligned according to the grid lines.[7] Heat conduction in the substrate defines the size of the pattern and thus limits the registration accuracy of the method.[8]

We report here a passivation process based on Joule heating. Instead of using a constant current for heating, as in our previous studies,[7–9] we used a pulsed current. The length of the pulse was selected not only to guarantee heating of the metal grid lines but also to minimize heat conduction into the substrate. This procedure is analogous to pulsed laser ablation, in which the size of the ablated area is limited using very short pulses. The typical pulse length is significantly longer than in laser ablation, on the order of milliseconds. Frequencies of this magnitude are not difficult to generate even in large volume production.

We present here a finite element simulation of the dependence of heating selectivity on pulse length and the experimental validation of the simulation. Finally, we demonstrate the feasibility of the process with excellent alignment accuracy of a passivated OLED anode grid on a glass substrate coated with Indium-tin oxide (ITO). The current distribution grids were printed to demonstrate the possibility of low-cost OLED manufacturing.

The registration accuracy of the Joule heating process depends on the spatial selectivity of the heating. Thus, by limiting the transfer of heat into the substrate through the use of short current pulses, we can improve the registration accuracy. The effect of pulsed heating on heating selectivity was studied by both model and experiment.

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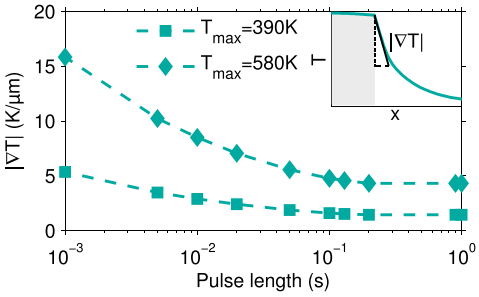

FIG. 1. Modelled effect of pulse length on the temperature gradient at the edge of the grid line at 390 K and 580 K in the conductor. Inset: Temperature profile from the center of the line to the substrate. The gray bar denotes the location of the grid line and the black line denotes the location where the temperature gradient is calculated.

The effect of the pulse length on heating selectivity was studied with a time-dependent thermo-electric model for a 500-nm thick silver line on polyethylene terephthalate (PET) substrate. The temperature gradient at the edge of the grid line was chosen as proxy for heat selectivity (results in Figure 1 with the temperature gradient and the profile from the center of the line to the substrate shown in the inset). The temperature gradient increases as the pulse length decreases. To have an effect on the localization, the heat pulse should be less than 0.1 s. Furthermore, an increase in the temperature increases the temperature gradient. Moreover, the higher the temperature, the more reducing pulse length increases the temperature gradient.

To verify the model data experimentally, we designed a silver line set with a current choke in the middle of the line (see inset in Figure 2) and evaporated it on a PET substrate. In the choke, the current density increases and induces a local rise in temperature. At a choke, higher temperature increases the overhang, since there is no corresponding decrease of curing time. Thus, the size of the dielectric overhang (x_{OH}) increases as the difference in line width (ΔW) increases. The increase depends on the heating selectivity in that the better the selectivity, the less the overhang increase. (See supplementary material for more detailed explanation.[10]) The experiments were run with 10-ms, 50-ms, 100-ms pulses and 1-min DC heating, and the increase in the dielectric overhang (Δx_{OH}) due to the choke was measured.

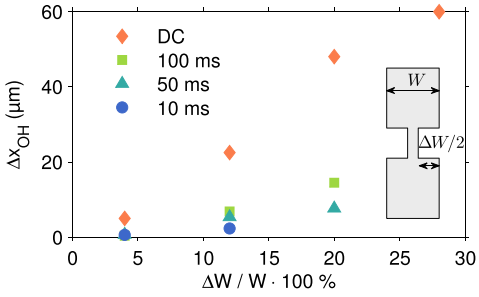

FIG. 2. The dielectric overhang (x_{OH}) increases when line width at the choke ($W - \Delta W$) decreases. As pulse length decreases, the size of the overhang is less prone to changes in line width.

As expected, the overhang increased when the difference in linewidth increased. When pulse length was decreased, the slope decreased, indicating a higher temperature gradient at the edge of the line. However, with very short pulse lengths, and corresponding higher peak power, the PET substrate melts at the narrow choke widths. We had fewer measurement points with the pulsed than with DC current, because the deformation of the substrate limited the size of the choke usable for experiments. For the same reason, the 50-ms and 10-ms experiments were done with 10 and 30 pulses, respectively, to be able to use lower temperatures and to avoid melting of the substrate, whereas with 100 ms only one pulse was used.

According to the simulation, increase in the temperature gradient should not be dramatic if pulse length is decreased from DC to 100 ms, whereas in the experimental data the selectivity increases significantly. This discrepancy results from the temperature induced at the line during Joule heating. With shorter heating, higher temperatures could be used without melting the substrate. As seen in Figure 1, the temperature gradient increases also as a function of temperature.

The optimal pulse length depends on the substrate used and the homogeneity of the target lines cross-sectional area. The better the thermal stability of the substrate, the more variation is allowed in the line cross-section without damage; furthermore, a shorter pulse length can be used. We emphasize here that the results in Figure 2 show a more dramatic increase in the overhang, and, moreover, the substrate melts with smaller differences in line width than expected in the passivation process. This is because the temperature in the choke increases as the length of it increases up to saturation. In the experiments, the length of the choke was chosen as 1 mm, which corresponds to the saturation length in constant current heating. Typically, the grid line cross-sectional area varies in length in tens of micrometers rather than in millimeters.

In addition to increased registration accuracy, pulse heating decreases energy consumption during curing. Table I shows the curing parameters and the energy consumed during curing for each Joule heating series. The pulse heating setup decreases the heat dissipated and lost in the substrate and cross-linking takes place faster at higher temperature, thus less energy was needed to cure the dielectric. With DC heating, energy consumption is three orders of magnitude greater than with pulsed heating. The required current increases when the pulse length decreases, but the pulse length and the total heating time are more markedly reduced. The lowest power consumption was achieved with a 100-ms pulse. Optimization of the pulse energy depends on the thermal stability of the substrate and the dielectric curing

TABLE I. Energy consumed during curing for all pulse lengths.

Sample	Current (mA)	Number of pulses	Total energy (J)
DC	320	1	27
100 ms	550	1	0.14
50 ms	550	10	0.68
10 ms	700	30	0.66

properties. In these experiments, the sample posed the limit for the maximum power level.

For a constant current Joule heating setup, glass is a challenging substrate material; accurately aligned dielectric patterns are difficult to produce due to its high thermal conductivity.[9] Pulse heating enables the use of substrate materials incompatible with DC heating, because it increases the registration accuracy. In addition to increased registration accuracy, a further advantage of pulse heating is that the curing time necessary for the polymer to cross-link decreases as the temperature increases. Cutting the process time from 1 min to 100 ms is significant and increases the attractiveness of the Joule heating approach as a method for high volume manufacturing.

In order to demonstrate the practical applicability of the pulsed Joule heating approach, it was used to passivate an OLED anode. Glass was selected as the substrate material, because it has better water barrier properties than PET. The anode electrode in the experiments was ITO with a sheet resistance of 10 Ω/□. The grid lines were 3-μm thick and approximately 90–μm wide printed silver lines. The separation of grid lines was 2 mm. A dielectric (Bectron AL14-018H from ELANTAS Beck) was cured using six 75-ms, 13-A pulse. A microscope image of a passivated grid line is shown in Figure 3(a). The registration accuracy of the process was excellent; the dielectric overhang was less than 5 μm, although linewidth varied from 80 μm to 100 μm.

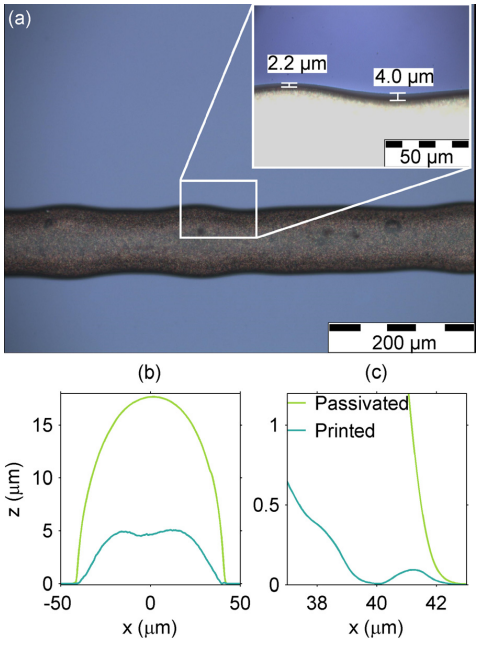

FIG. 3. (a) Microscope image of an evaporated grid on an ITO coated glass substrate passivated using a pulsed Joule heating setup. (b) Profile of the printed line with and without passivation layer. (c) Magnification of the edge of the line profile. Note that the linewidth of the printed line is not constant and the images are not taken from the same location of the line.

Figures 3(b) and 3(c) show the height profiles of a printed line with and without passivation layer, measured with a stylus profilometer (Veeco Dektak 150 Surface Profiler). The passivation layer smoothens the surface of the printed line resulting in a RMS roughness value of 5 nm on the line. The passivation layer is relatively thick, about 13 μm, though the size of the overhang is only few microns.

The characteristic IV curves for an OLED reference and an OLED with grid lines passivated with the method described above are given in Figure 3, where the inset is an image of the OLED with current distribution grid. Electrical losses in this non-light-emitting voltage range are an indication of irregularities in the electrical field between anode and cathode. Contributions to these loss channels can be found in a rough surface topology[11] or the migration of silver ions. These effects reduce the reliability of the device. The non-emitting voltage range between 0.5 and 2 V is highlighted by dashed lines. The leakage current in this range is of a comparable order of magnitude for devices with passivated grid lines and for the reference device without grid lines. Therefore, it can be concluded that the surface topology of the substrate allows for reliable operation of OLED devices and that the dielectric passivation effectively covers the Ag lines. Water vapor residues outgassing from the passivation lines deteriorated the OLED stack in the vicinity of the grid lines (closer than 100 μm) in the form of blurred blackish artifacts, as can be seen in the inset of Figure 4. To remove this water contamination, another, hydrophobic, polymer should be used.

The size of the OLED active area was relatively small compared with the high conductivity of ITO. Thus, more significant improvement in IV characteristics of the device with grid could be shown with devices having less conductive transparent electrode, larger active area, and optimized line pitch.[12–14]

In this study, we introduced a pulsed-Joule-heating-based passivation method for OLED anode grid lines. Instead of a constant current for heating, as in our previous studies,[7–9] we used a pulsed current to limit heat conduction into the substrate and polymer layer. We have shown both theoretically and experimentally an increase in heating

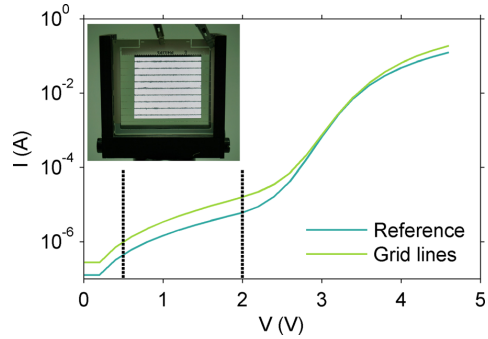

FIG. 4. IV-curves of a reference OLED and an OLED with current distribution grid (size of the active area 900 mm^2). Inset: Photograph of an OLED with current distribution grid under operation.

selectivity as pulse length decreases. Heat conduction defines the selectivity of the heating, which is the key parameter for the registration accuracy of the process: the less heat is conducted into the substrate, the better the registration accuracy. Our method extends the selection of substrate material compatibility with Joule heating from plastic to thermally more conductive glass substrates. The registration accuracy we achieved on an ITO-coated glass substrate was better than 5 μm, which is comparable with registration accuracy of roll-to-roll photolithography for well-defined target lines. Furthermore, variations in line width had only a slight effect on the accuracy. In addition, pulse heating helps reduce process time and energy consumption significantly over constant current heating. In conclusion, the scalability of the method for high volume manufacturing improves in the following parameters: process time, registration accuracy, and material selection. We demonstrated the compatibility of the concept for evaporated OLED stacks.

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Publication V

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